

TIMEX COMPUTER 2048

Service Manual



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TIMEX

TC 2048

**SERVICE
MANUAL**

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Introdução e Descrição do Sistema

Este manual é destinado a técnicos, engenheiros e representantes autorizados pela T.M.X-PORTUGAL como um guia para a reparação do Computador pessoal TC 2048.

Considera-se que para este efeito, as pessoas que irão desempenhar essa função, tenham alguns conhecimentos de electrónica e porventura alguma experiência na reparação de Microcomputadores. O manual refere especialmente os ISSUE 4B e 5A, mas contém informações sobre os primeiros Boards assim como um historial sobre as principais modificações implementadas desde o primeiro ISSUE. O TC 2048 é um Microcomputador cujas características técnicas foram substancialmente melhoradas obtendo assim uma nova performance comparativamente com outros microcomputadores da sua gama, por exemplo o ZX SPECTRUM.

Uma das inovações em Hardware, é a utilização de uma nova tecnologia de RAM'S de 16K por 4 Bits alimentadas apenas por uma tensão de +5 Volts, isto implica uma redução no número de IC'S (23 para 16), assim como o consumo de corrente e a dissipação de calor se tornam menores.

Outra das novidades é a incorporação de um PORT para Joystick, uma saída de VIDEO para monitores Monocromáticos, bem como uma melhoria na qualidade e volume de SOM. Possui ainda um interruptor POWER ON/OFF com o respectivo LED indicador.

Este microcomputador é constituído por um Z80 de 8 bits a 3.5MHZ de Clock, uma SCLD que gera o RGB-SYNC, para Video, controle de Teclado, Multiplexagem e Seleção das Memórias e os PORTS TAPE de entrada série (EAR) e saída (MIC) com o sinal incluído bem como uma ROM de 16K e 48K de RAM.

O teclado é do tipo rígido constituído por um circuito impresso onde está implementado a matriz do teclado, sendo os contactos efectuados por pastilhas de borracha condutora. A interligação do teclado é feita através de um "Flat-Cable" & "Mather Board".

Organização da Memória

Quanto à organização da memória, os primeiros 16K (endereço 0000-3fff) estão ocupados pela ROM (IC3) que contém o programa Monitor.

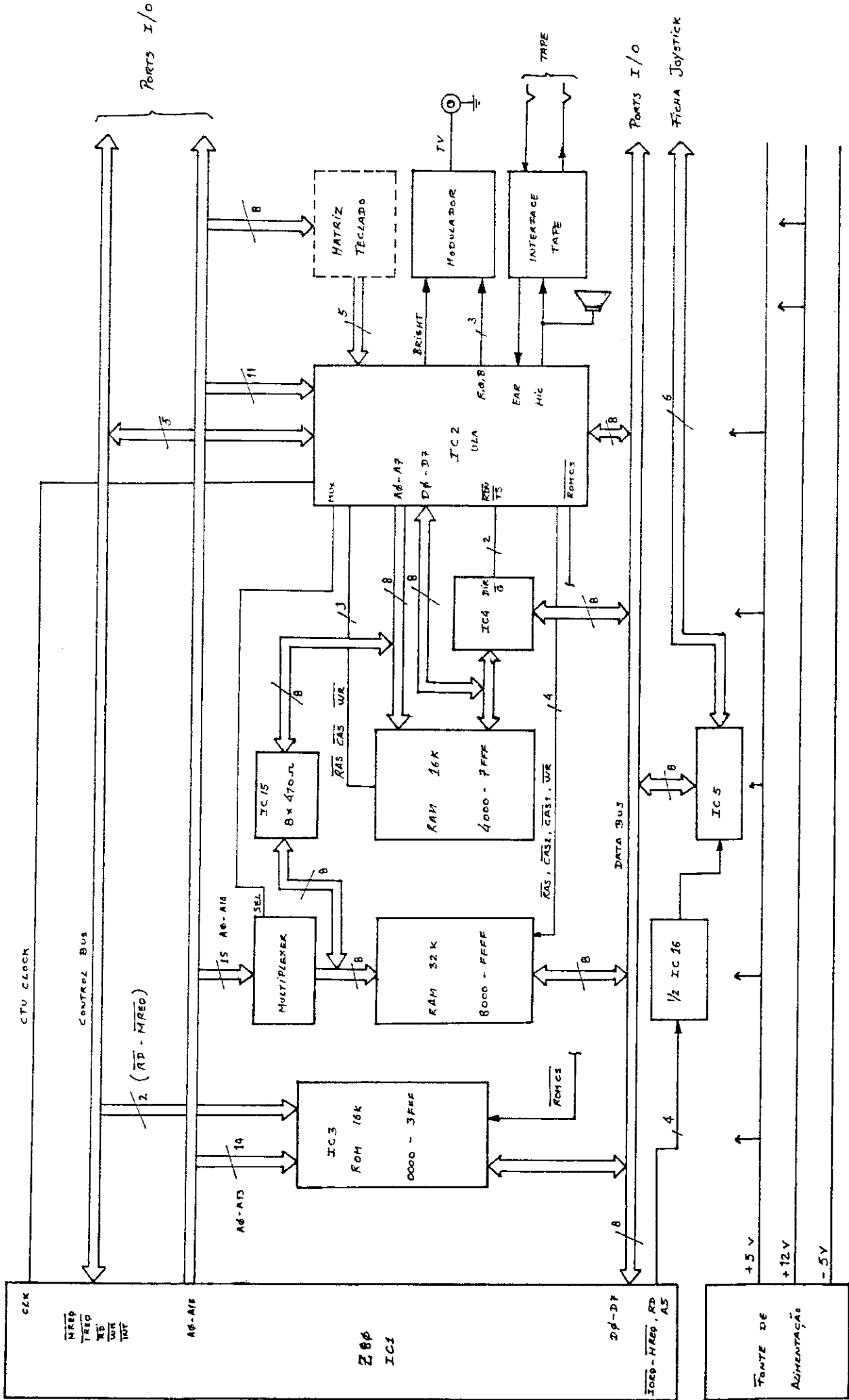
Este micro, está preparado para levar diversos tipos de ROM (NEC HITACHI,61 e EPROM 27128) sendo seleccionadas através dos jumpers LK1,...LK7 que se encontram situados no lado direito .

Os seguintes 16K de memória (endereço 4000-7ffff) são utilizados pelos IC 6,7. Do endereço 16384 a 22528 ocupam uma parte de memória destinados para o Display File.

Por último temos o banco de 32K de RAM (endereço 8000-ffff) ocupados pelos IC 8,9,10,11. Na versão de ISSUE 5, o banco de 32K é ocupado pelos IC8 e IC9 (41464 ou 41254) e a ROM passa a ser uma EPROM 27128.

Os IC13 e IC14 fazem parte da organização dos 32K de Memória são ambos Multiplexer's de 8 Inputs para 4 Outputs não inversores.

DIAGRAMA DE BLOCOS



Circuito de Alimentação

=====

O Circuito de Alimentação, tem incorporado um Regulador de Tensão "7805", sendo o componente principal, uma vez que alimenta o computador com uma tensão estabilizada de +5 Volts.

Esta tensão está protegida contra curto circuitos.

O Circuito de Alimentação, além do Regulador de Tensão é constituído por um outro circuito que fornece os +12 Volts para o circuito de C&R, e pelo circuito dos -5 Volts e 12Volts AC.

Podemos agora descrever o funcionamento do circuito de alimentação.

Como atrás já foi mencionado, o regulador de tensão (7805) reduz a tensão de entrada (+9VDC) para +5 VDC. A mesma tensão proveniente da fonte de alimentação exterior (Jack 1), alimenta o circuito " oscilador, elevador de tensão ", constituído pelo transformador "L1", C21, R51,52, e Q1.

O transistor Q1, entra em corte e saturação, devido ao condensador C21, tendo as resistências R51,52, como função de limitar a tensão de base do transistor. Uma vez que o circuito se encontra a oscilar, a tensão em "L1" é elevada para 14 VAC, indo directamente para o Edge Connector, e ao mesmo tempo alimenta o circuito de 12 VDC, e -5 VDC.

No circuito de + 12 VDC, constituído pelos diodos D11,12,13,14, 18, e o condensador electrolítico C22, a tensão 14 VAC, é rectificadada pelos diodos D11,12, sendo depois estabilizada pelo diodo zenner de 12 Volts -D18-, e pelo condensador C22.

Esta tensão é dirigida depois para o circuito de C&R através da resistência R48, que tem como função limitar e proteger os 12V para o circuito a que se destina. Esta tensão também é dirigida para o Edge Connector.

A extracção dos -5 Volts, é feita através do condensador C23 que recebe a tensão não estabilizada de 14 VAC e invertea em relação à massa. Por sua vez, esta tensão é rectificadada e estabilizada pelos diodos D15,16 e pelo condensador C24. Esta tensão faz-se passar pela resistência limitadora R53, sendo estabilizada a -5 Volts através do componente seguinte, que é um Zenner de 5V1 -D19-.

Nota:

Nos computadores TC2048 Issue 5, existe um circuito adjacente ao circuito dos -5V, que tem como função melhorar o tratamento do sinal no circuito de EAR. Este circuito é constituído pelos componentes R21,22 e C53 que reduzem e estabilizam a tensão de - 12V para - 700 Milivolts.

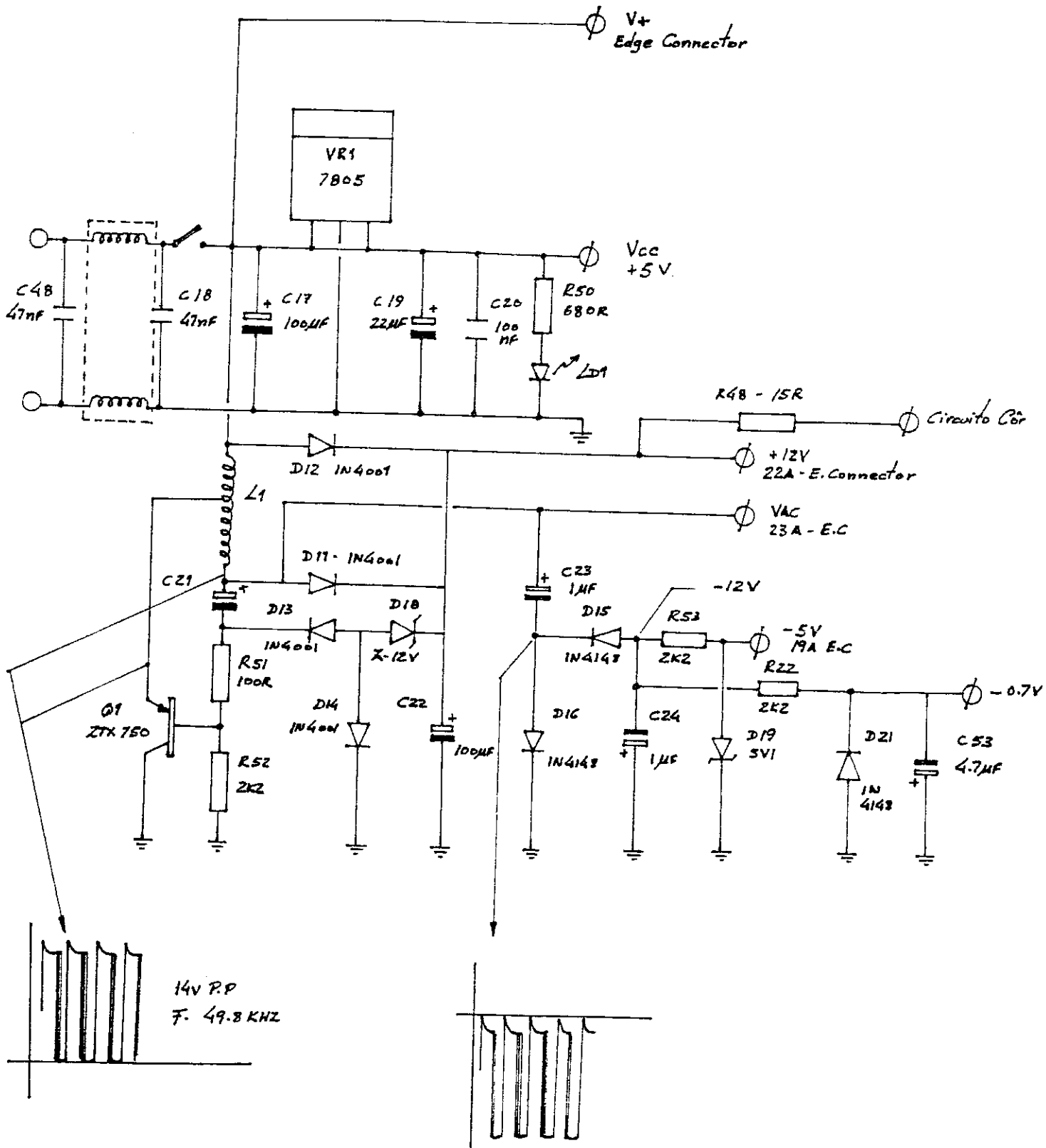
Em modos normais de funcionamento, o circuito "oscilador elevador" funciona a uma frequência de 49.6 KHZ.

Sempre que é ligado um periférico no Edge Connector com o Computador ligado, existe sempre uma sobre carga no circuito de 12V AC, obrigando por isso uma passagem de corrente excessiva no transistor obrigando-o a entrar em rotura.

Uma vez que isto acontece, o computador deixa de ter CDr e existe ausência das tensões de -5V e 12VAC no Edge Connector.

Acontece porém, o transistor se encontrar a oscilar e não haver os + 12 Volts, sendo assim verifique o diodo zenner D18 e os diodos D11,12,13.

Quando estamos na ausência dos -5V, e o primeiro circuito se encontra a oscilar, verifique o diodo zenner 5V1 -D19-, e o diodo D15.



Funcionamento e Características da Power Supply TC 2048

A Fonte de Alimentação exterior ao Computador, é constituída por um Transformador com as características abaixo descritas, por quatro diodos (1N 4001), que rectificam a tensão AC para DC e por dois condensadores electrolíticos de 4700UF/16V que estabilizam e suprimem o Reaple da tensão rectificada.

Características do Transformador:

Input -- 202 VAC -- 50 HZ --
OutPut - 8.5 VDC a 800 Miliamperes com uma tensão de pico de 9 Volts, e tensão mínima de vale 8 Volts.

Input -- 220 VAC -- 50 HZ --
OutPut - 9.5 VDC a 800 Miliamperes com uma tensão de pico de 10 Volts, e tensão mínima de vale 9 Volts.

Input -- 238 VAC -- 50 HZ --
OutPut - 10.5 VDC a 500 Miliamperes com uma tensão de pico de 12 Volts, e tensão mínima de vale 10 Volts.

Circuito de Cr

=====

O circuito de cr  baseado no funcionamento do IC12 (MC377- Codificador R.G.B - PAL/NTSC), sendo este um dos componentes principais do circuito.

A ULA (SCLD) U2, gera quatro sinais importantes para que se possa ter cr, sendo eles: R,G,B e o Sinal de Sincronismo Composto (Sincronismo de Quadro e Sincronismo de Linha - Freqncia de 15.625KHZ + 50HZ).

Com a presena destes quatro sinais nos pinos 2,3,4,5 do IC12 obtemos o sinal de Video  sada do pino 9 do mesmo. Este sinal Composto  por sua vez atenuado pela malha R44,45 e inserido directamente na entrada do Modulador UHF (Standard Europeu Canal 36), que depois ir permitir-nos a Visualizao no Televisor a Cr ou a Preto/Branco.

Esta combinao, produz uma resoluo de 24 Linhas por 32 Caracteres com a incluso das oito cores (Preto, Azul, Vermelho Magenta, Verde, Cyan, Amarelo e Branco).

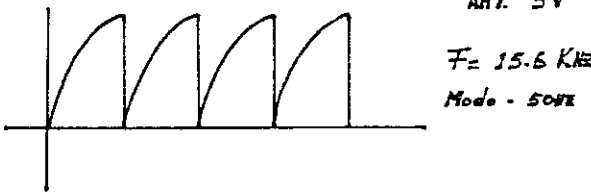
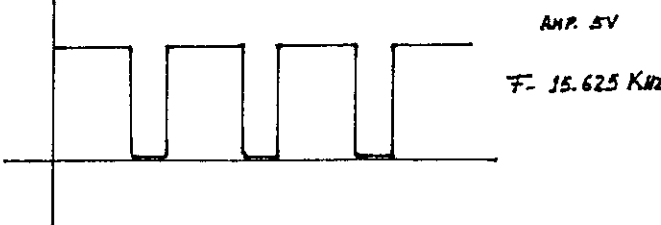
O MC 1377, tem uma sada (Pino 20) que define a Freqncia do seu funcionamento (50/60HZ), assim como o Cristal X1 (Cristal da Cr); tambm varia de valor consoante o Sistema a utilizar:

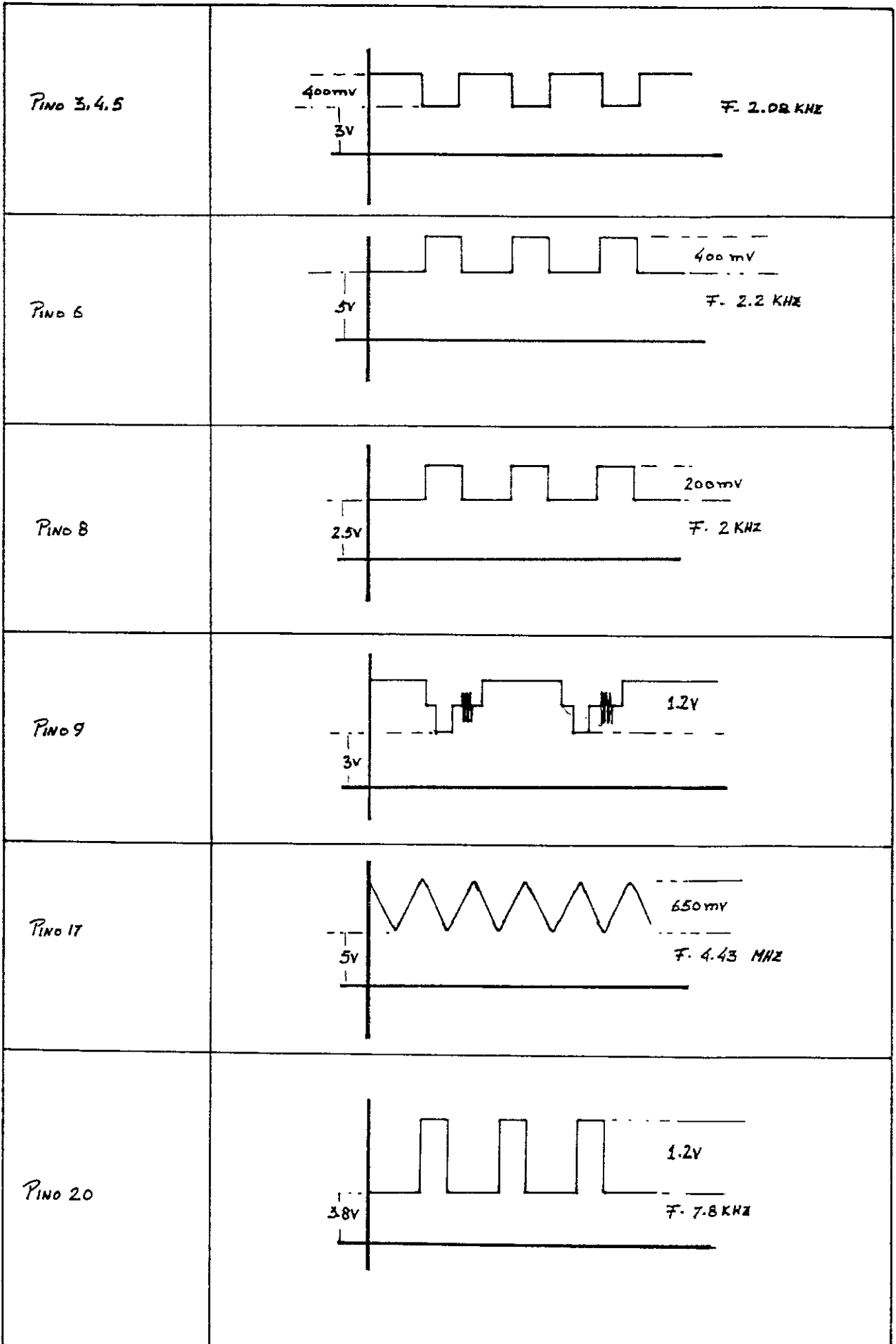
Freqncia da Rede 50HZ ----- No leva Shunt em LK2
 " " " 60HZ ----- Leva Shunt em LK2

Sistema a Operar:

PAL M ----- Cristal X1 3.5756611 MHZ
 PAL N ----- " " 3.5820 MHZ
 PAL B/G ----- " " 4.431619 MHZ
 NTSC ----- " " 3.579545 MHZ

— MC 1377 —

PINO N	SINAL
PINO 1	
PINO 2	



SINTOMA	ANALISE	LOCAL DA AVARIA
Ausência de SCREEN	-Frequência no Modulador Desajustada (Ajuste na Bobine com o auxílio de chave apropriada) -Ausência de alimentação no Modulador (+5 Volts) -R44,R45 em aberto/valor alterado.	Modulador R43,P.Supply
Ecran com " Chuva "	-Verificar os sinais nos pinos 2,3,4,5 de U12. -Ausência de sinal no pino 9 de U12. -Ausência de sinal no pino 17 de U12.	MC 1377 " " X1
Ecran com Interferências.	-Verificar os diodos D11 D12. -Verificar R48	Swicthing
Ecran com Faixa Escura em Movimento Vertical.	-Verificar os diodos D11 D12,D13. -Verificar se o transistor Q1 se encontra a oscilar. -Verificar L1.	"
Ecran Escuro com Logotipo não Visível.	-Verificar o sinal de Sincronismo & saída de U2	U2
Ecran Escuro com Falta de Sincronismo	-Verificar os sinais nos pinos 2,8,9,16 de U12.	U12
Ausência de BRIGHT	-Verificar os sinais R/G/B à saída de U2. -Verificar os diodos D9,10 - " Q3 -Verificar saídas de U16 -U2 com anomalia	- U2 - - U12 - - U16 - - U2 -
Ausência Total de Cor	-Verificar a tensão + 12V -X1 avariado -Ausência de R/G/B -Verificar C32,C33 -L2 em Aberto -Verificar C42,43,45,46	Swicthing - X1 - - U2 - -U12 - - " - - " -

Ausência das Cores Verde/Vermelho Magenta.	-Verificar C35 -R30 em Aberto/Valor Alterado. -U12 Avariado -U2 Avariado	-U12 - - " - - " - - U2 -
Ausência das Cores Cyan/Amarelo/Branco	-Verificar C36 e R29 -U12 Avariado -U2 Avariado	-U12 - " - U2 -
Ausência das Cores Azul/Magenta/Branco	-Verificar C37 e R28 -U12 Avariado -U2 Avariado	-U12 - " - U2 -
Ausência de Cór com Coluna Escura no Ecran	-D42 com valor alterado ou em Aberto	-U12 -
Ecran dividido em Cores Verde/Vermelho	-D43 com valor alterado ou em Aberto.	-U12 -
Ecran com Imposição da Cór Azul.	-Verificar o Sinal -R- & saída de U2.	- U2 -
Ecran com Imposição das cores Vermelho e Magenta.	-Verificar o sinal -G- & saída de U2.	- U2 -
Ecran com Imposição da Cór Amarela.	-Verificar o sinal -B- & saída de U2.	- U2 -
Ecran com Brilho Intenso	-D9 em Ruptura	- U2-U12-

Circuito de Video

=====

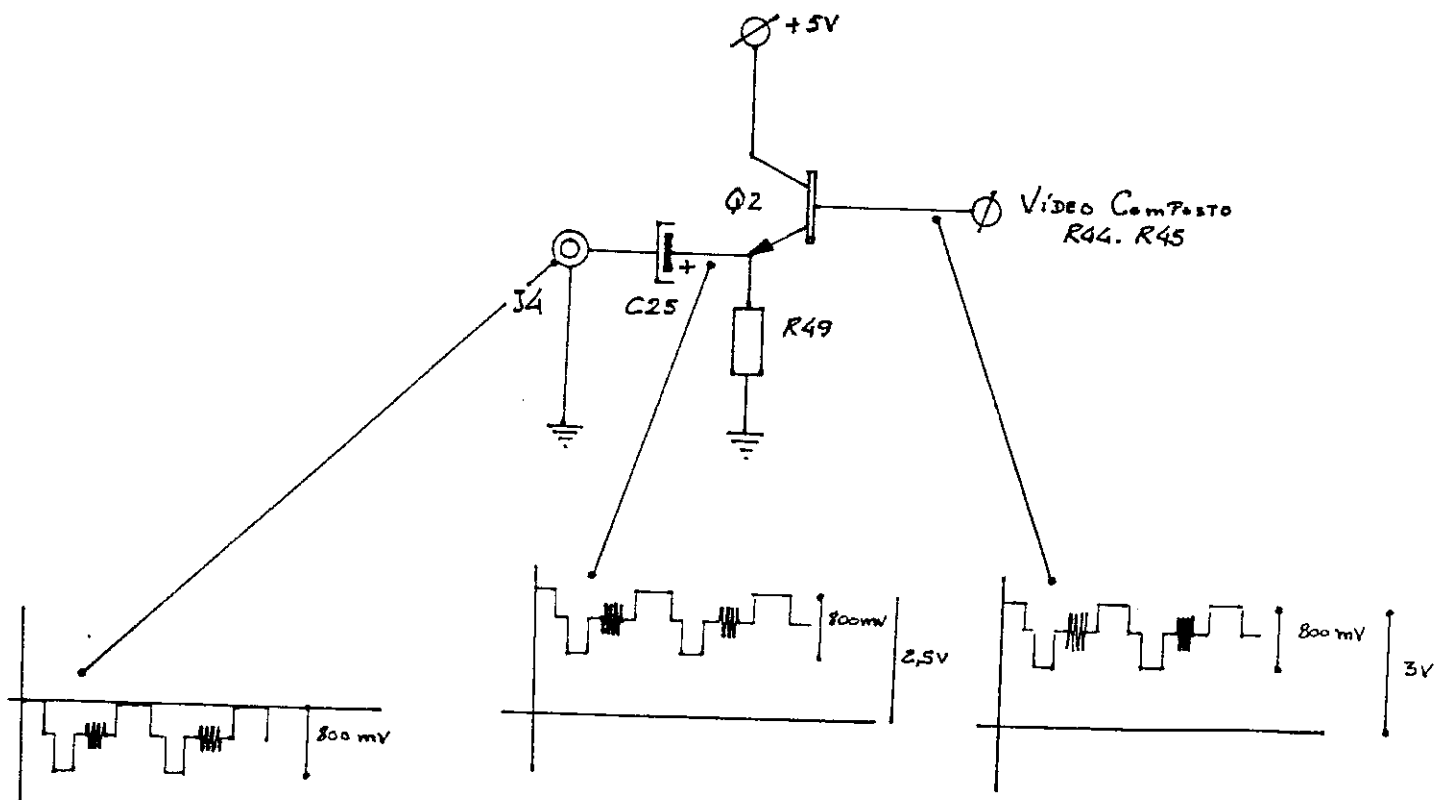
O circuito de Video é constituído pelo Transistor Q2, Condensador Electrolítico C25 e pela resistência R49.

A descrição de funcionamento do circuito, baseia-se na extração do sinal Video Composto da entrada do Modulador (MD1) através da malha R44, R45, e injectá-lo directamente na base de Q2 que se encontra montado em Modo Emissor Comum. A função do transistor, não é mais do que um " Drive " à saída do sinal sendo este Desacopulado em DC através do condensador C25, e atenuado pela resistência R49.

Quando se utiliza um Monitor, e estamos na Ausência de Sinal (Ecran do Monitor Escuro), deve-se verificar o mesmo há saída do Jack (J4), e comparar com a Fig. abaixo descrita. Existem quatro avarias definidas para este tipo de avaria:

- 1.1- Falta de alimentação (+5V) no Colector de Q2.
- 1.2- Ausência de Sinal Video Composto na Base de Q2.
- 1.3- Transistor Q2 em Rotura.
- 1.4- Condensador C25 com valor alterado ou com defeito interno

Nota: Quando estamos na ausência de Sinal na Base de Q2, também não temos Imagem no Televisor, (Consulte a descrição e Funcionamento do Circuito de Cor).



Estrutura do Teclado

=====

A estrutura do teclado define-se numa Matriz de Dito por Cinco. Os oito pontos da matriz, encontram-se ligados a 8 diodos (D1, - a D8) que por sua vez estão conectados às 8 linhas de Address Bus (A8, ... A15). Os restantes 5 pontos da matriz ligam directamente à SCLD U2 nos pinos 3,4,5,6 e 43.

Matriz do Teclado

=====

!	C.Shift	!	Z	!	X	!	C	!	V	
*	-----	*	-----	*	-----	*	-----	*	-----	D1
!	A	!	S	!	D	!	F	!	G	
*	-----	*	-----	*	-----	*	-----	*	-----	D2
!	Q	!	W	!	E	!	R	!	T	
*	-----	*	-----	*	-----	*	-----	*	-----	D3
!	1	!	2	!	3	!	4	!	5	
*	-----	*	-----	*	-----	*	-----	*	-----	D4
!	6	!	7	!	8	!	9	!	0	
*	-----	*	-----	*	-----	*	-----	*	-----	D5
!	Y	!	U	!	I	!	O	!	P	
*	-----	*	-----	*	-----	*	-----	*	-----	D6
!	H	!	J	!	K	!	L	!	Enter	
*	-----	*	-----	*	-----	*	-----	*	-----	D7
!	B	!	N	!	M	!	S.Shift	!	Space	
*	-----	*	-----	*	-----	*	-----	*	-----	D8
!	KBO	!	KB1	!	KB2	!	KB3	!	KB4	

D1, ... D8 ----- ADDRESS BUSS

KB1, ... KB4 --- SCLD (U2)

Avarias de Teclado

=====

SINTOMA	ANALIZE	LOCAL DA AVARIA
Dificuldade na tecla para que a ins- trução entre.	Verifique a zona de con- tacto que deve estar com indícios de Oxidação.	Zona de Contac- to da tecla em causa (PCB).
Falha nas teclas C,S,Z,...V	Verifique a Junção do Diodo D1	Diodos junto à Ficha CN2
Falha nas teclas A,...G	Verifique a Junção do Diodo D2	"
Falha nas teclas Q,...T	Verifique a Junção do Diodo D3	"
Falha nas teclas 1,...5	Verifique a Junção do Diodo D4	"
Falha nas teclas 6,...0	Verifique a Junção do Diodo D5	"
Falha nas teclas Y,...p	Verifique a Junção do Diodo D6	"
Falha nas teclas H,...Enter	Verifique a Junção do Diodo D7	"
Falha nas teclas B,...Space	Verifique a Junção do Diodo D8	"
Falha nas teclas pertencentes a um Bloco de 2 Colunas	SCLD Avariada	U2
Falha em teclas Alternadas	Verifique o Contacto do Flat-Cable nas Fichas	Ficha CN2 Ficha Teclado

Teste do Banco de Memória de 32K

=====

Quando se liga o TC2048 " Power On ", este microcomputador possui uma característica ao Inicializar, que nos é possível identificar através das imagens sucessivas no Ecran do Televisor ou Monitor, até que surja o respectivo Logotipo " Sinclair Research, ... ".

Pois esta característica está no tempo da sucessão das imagens a primeira é mais rápida que a segunda.

Se o TC2048 possuir uma avaria no Banco de 32K, é possível ser detectada por duas maneiras. A primeira é pelo tempo da Inicialização como já foi mencionado, e a segunda a partir do RAM-TOP da memória.

Exemplo: Introduza a seguinte instrução

PRINT PEEK 23732 + 256 * PEEK 23733

O valor obtido terá de ser 55535 correspondente ao último endereço de Memória válida.

Se o valor obtido for diferente, significa que é no endereço seguinte onde se encontra a FALHA. Deste modo pode-se identificar qual das Ram's do bloco de 32K se encontra avariada.

Exemplo: Se o valor obtido for 32767, significa que todo o bloco de 32K se encontra inoperacional devido à existência de um endereço não reconhecido na primeira Ram U9 possuidora dos quatro Bits Menos Significativos.

Assim para determinar a localização do erro execute as seguintes funções:

POKE 32768,85 : PRINT PEEK 32768

POKE 32768,170 : PRINT PEEK 32768

Se os valores obtidos não correspondem a 85 e 170, consulte a tabela abaixo descrita.

DATA " 85 "	DATA " 170 "	BIT ERRADO	RAM	AVARIADA
			<49151	>=49151
84	171	0		
87	168	1	U9	U11
81	174	2		
93	162	3		
69	186	4		
117	138	5	U8	U10
21	234	6		
213	42	7		

Análise e Reparação do TC 2048

=====

Quando o TC2048 é ligado (Power On), ele executa em directo o Ciclo de Inicialização escrevendo a mensagem " 1982 Sinclair Research.

O ciclo compõe-se de três partes que são as seguintes:

- 1- Obtém-se no Ecran, um Paper escuro com barras alternadas de Azul e Vermelho.
- 2- O Paper figura-se de uma cor escura que se enche gradualmente com barras verticais, fazendo o CLEAR do ecran seguinte.
- 3- O Paper e o Border ficam da mesma cor (Branco) aparecendo a Mensagem escrita no Ecran.

Quando o computador se encontra avariado, geralmente fica bloqueado no primeiro ou segundo Paper nunca chegando a completar o ciclo devido a uma falha no BUS de DADOS, BUS de ENDERECOS ou nas linhas de Comando (Sistema, CPU ou Bus).

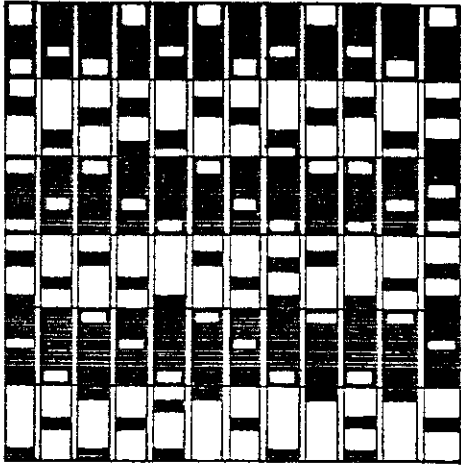
As figuras abaixo descritas facilitam ao reparador o modo mais rápido de chegar ao local da avaria.

Equipamento Necessário para a Reparação do TC 2048

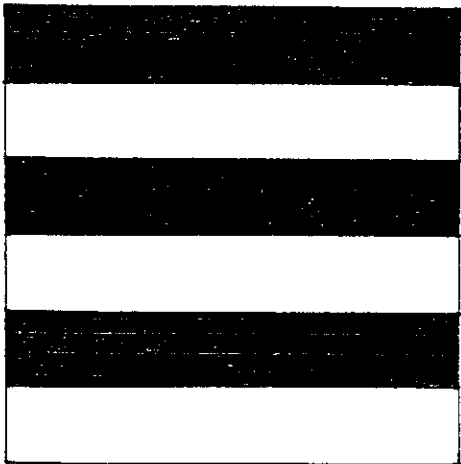
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Para se proceder à reparação do TC 2048, é necessário dispor-se do seguinte material:

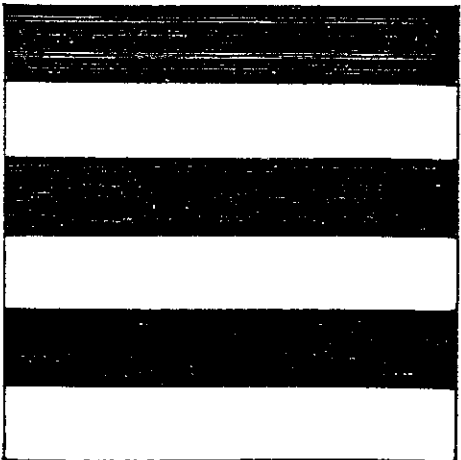
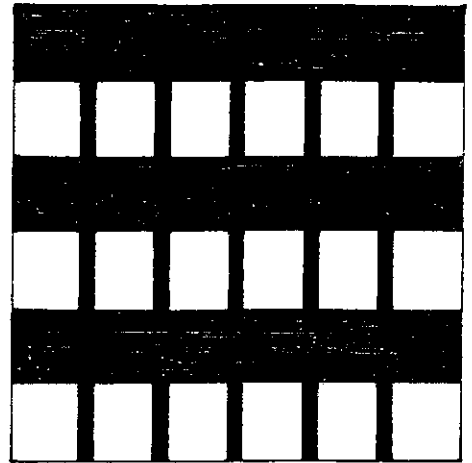
- 1- Fonte de Alimentação (Power Supply 2048).
- 2- Televisor a Cores.
- 3- Monitor Monocromático.
- 4- Osciloscópio de 20 MHz (ou superior) de Duplo Traço com Pontas de Prova #10.
- 5- Multímetro de preferência Digital (3, 1/2 Dígitos).
- 6- Ferro de Soldar e Ferro de Dessoldar preparados com funcionamento Anti-Estático.
- 7- Leitor/Gravador de Cassetes.
- 8- Cabos de Ligação (TV, Monitor, Ear/Mic).
- 9- Eprom de Teste TC 2048.
- 10- Ferramenta Miniatura (Alicates de Corte, Pontas, etc...)



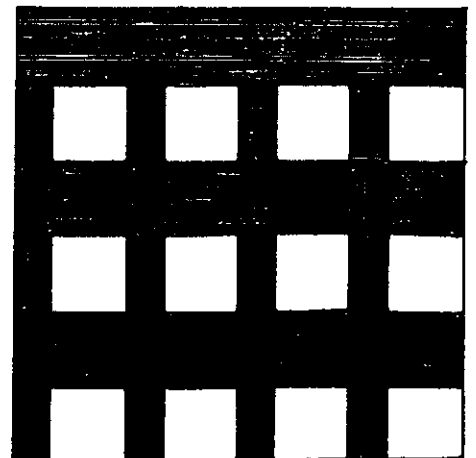
— AO —



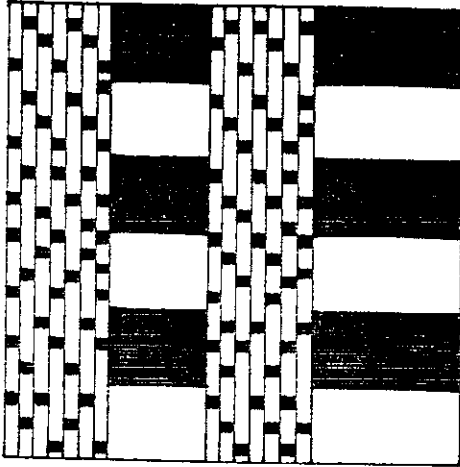
-- A1 --



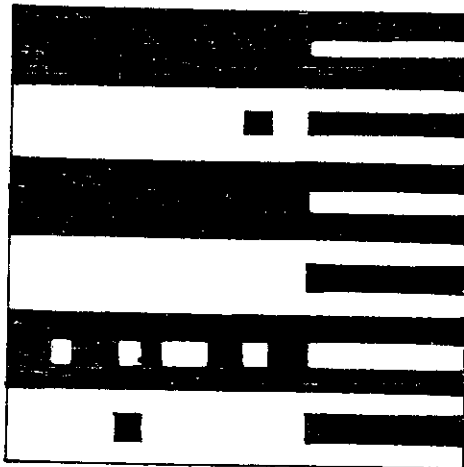
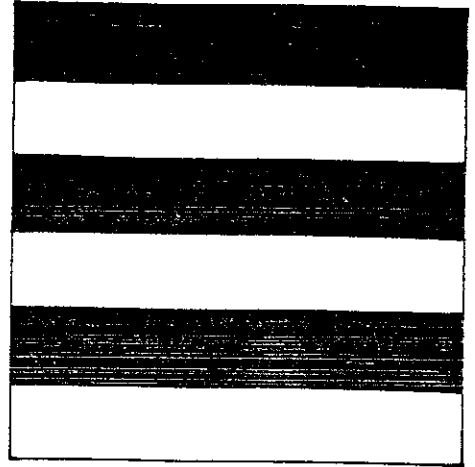
-- A2 --



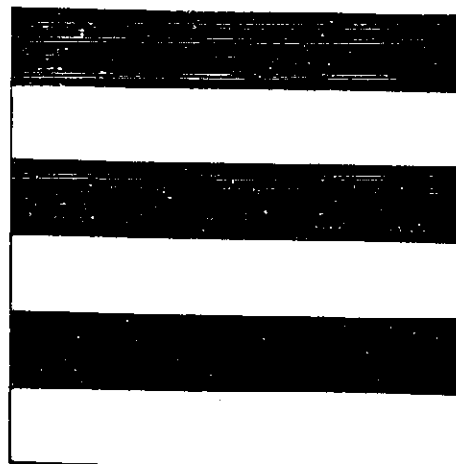
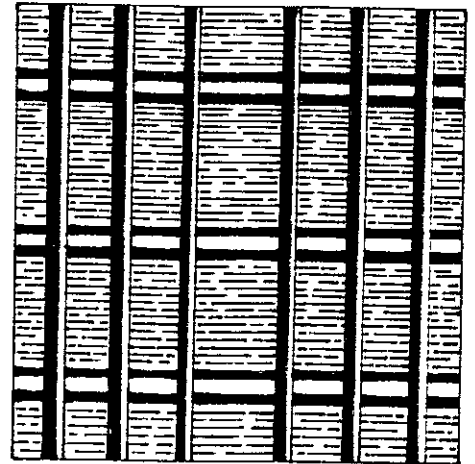
-- A3 --



-- A4 --

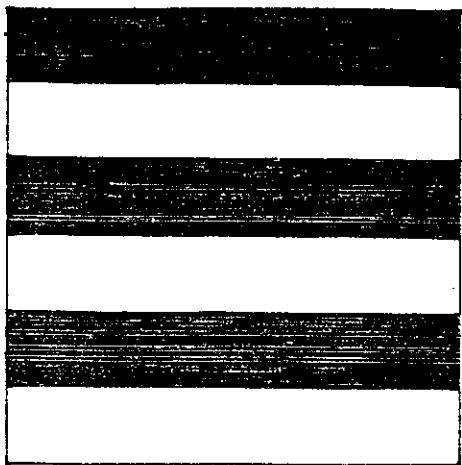


-- A5 --

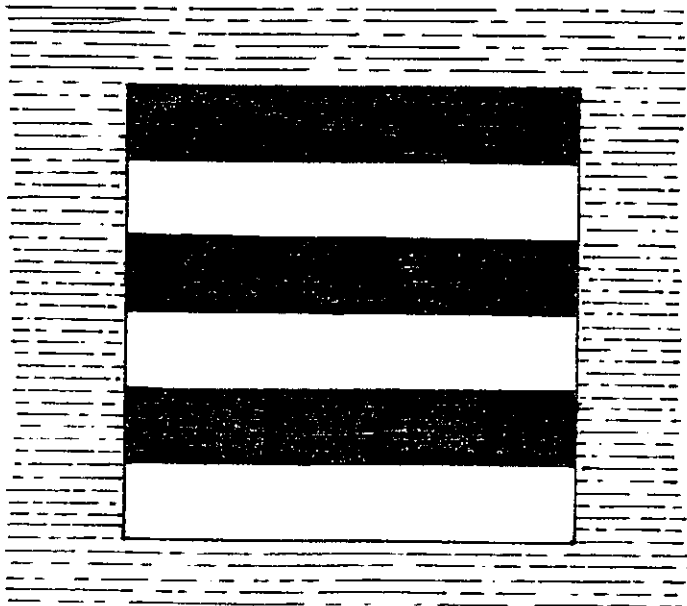
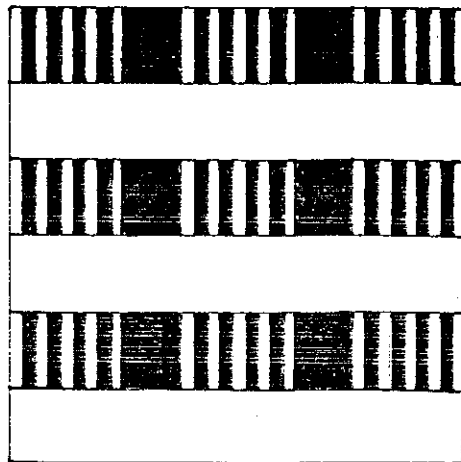


-- A6,A14--

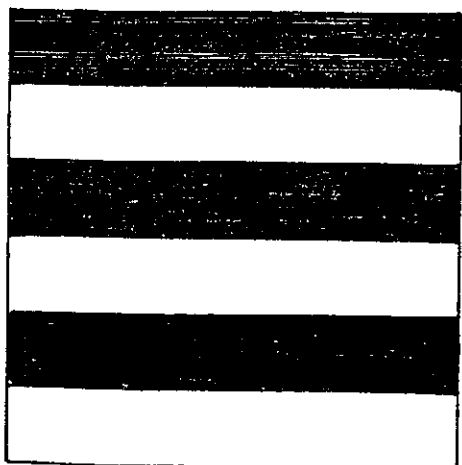
-- D0,D1,D2,D3,D4,D6,D7 --



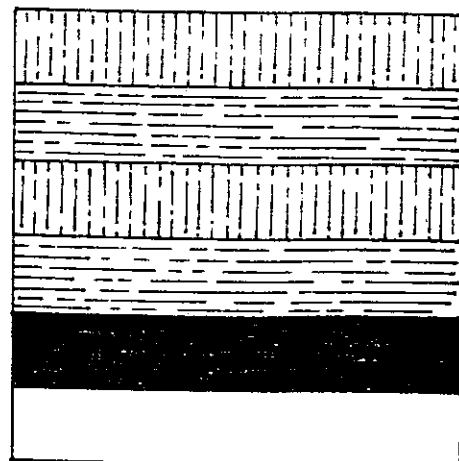
-- A7 --

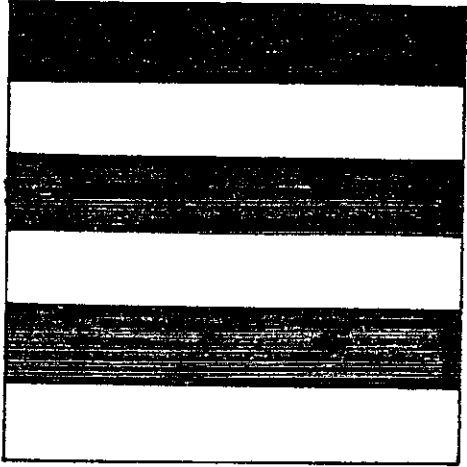


-- A8,A11 --

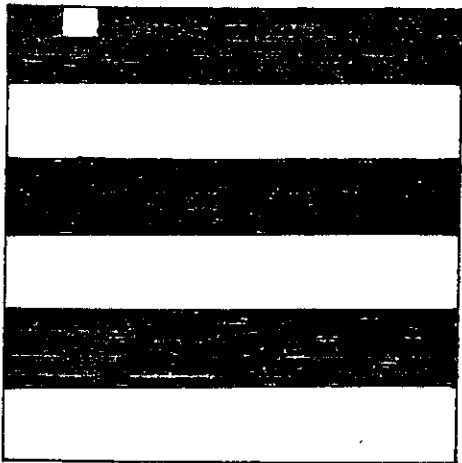
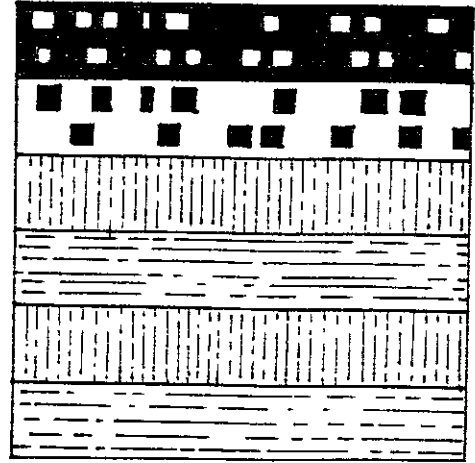


-- A9 --

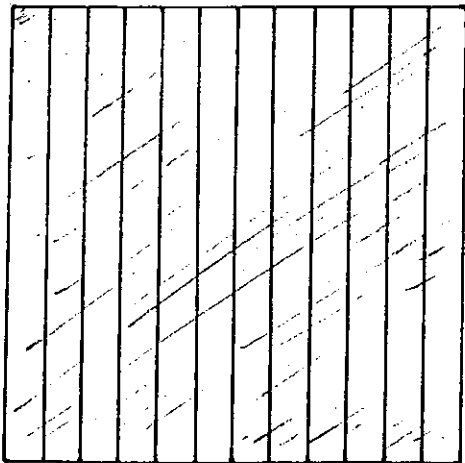




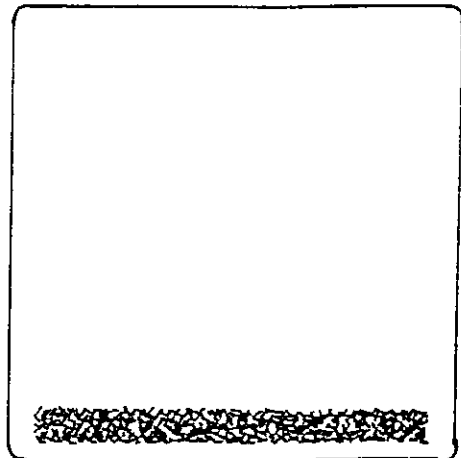
-- A10 --

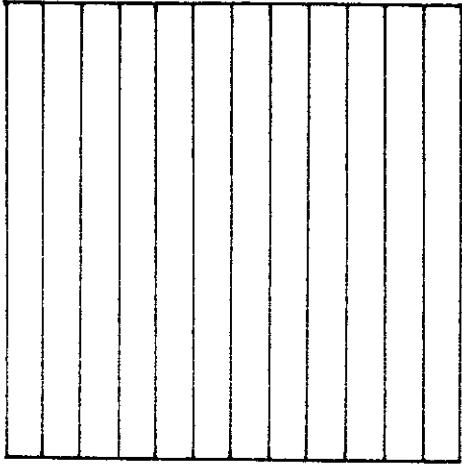


-- A12 --

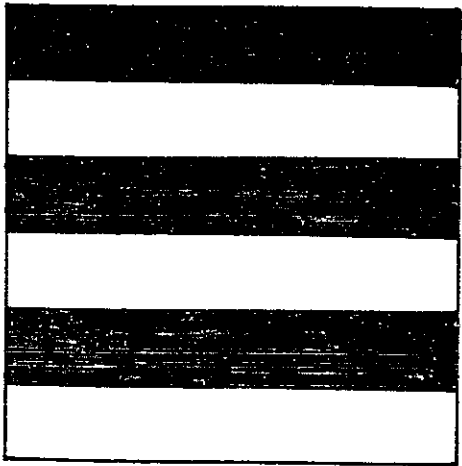
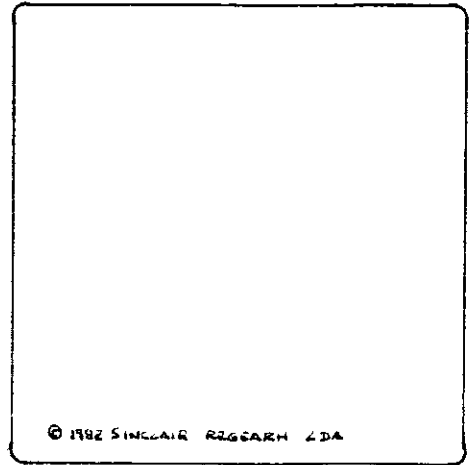


-- A13 --

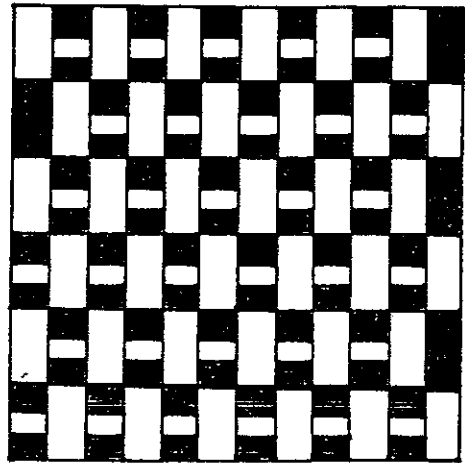




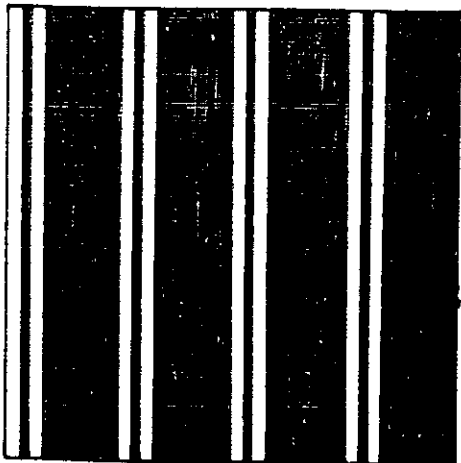
-- A15 --

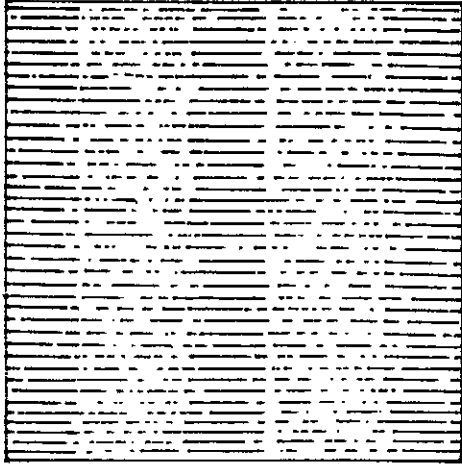


-- D5 --

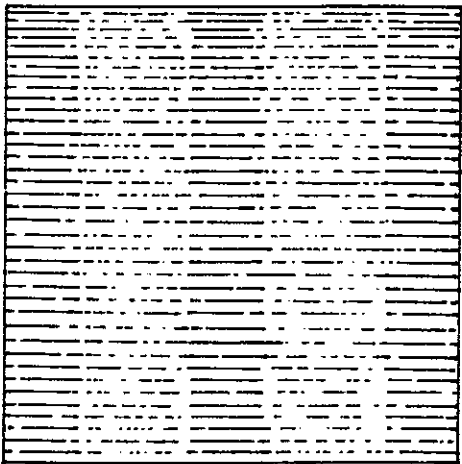
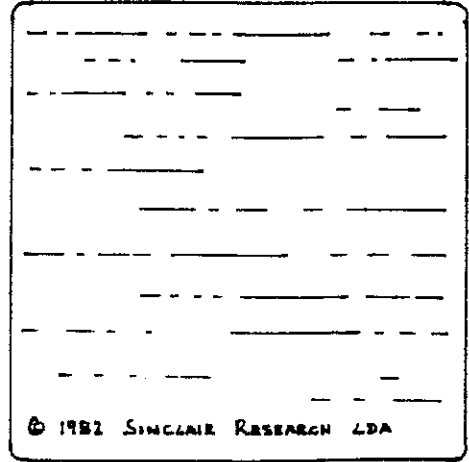


-- ROM --

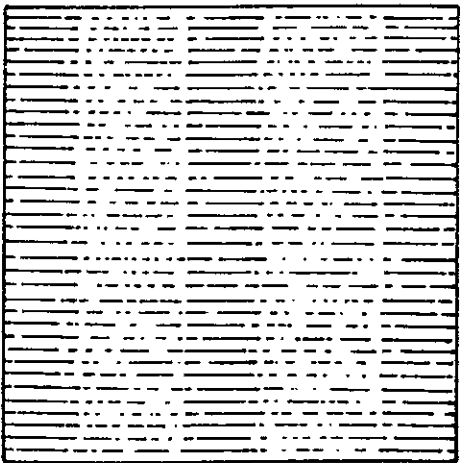
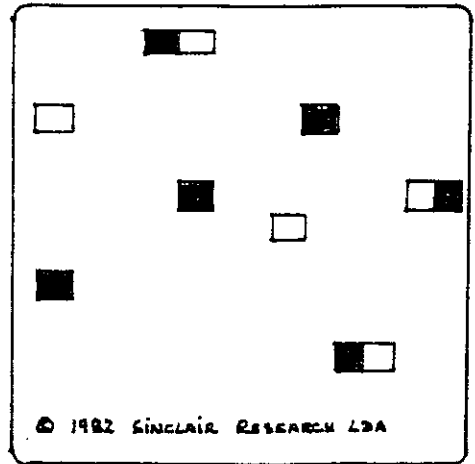




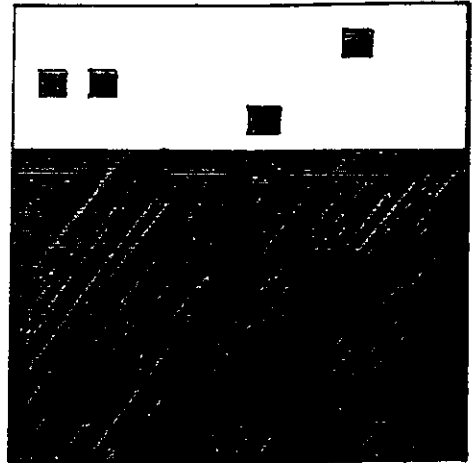
CAS
-1-

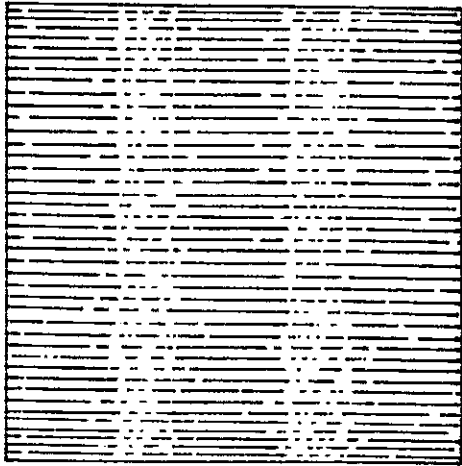


-2-

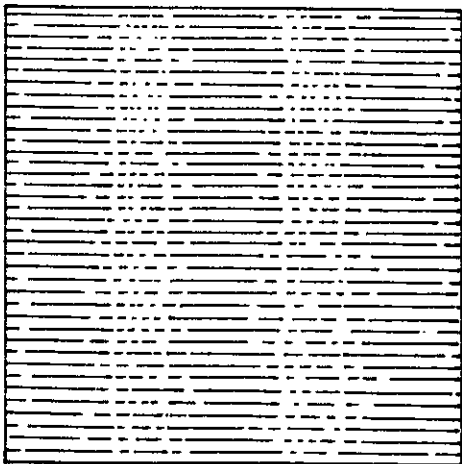
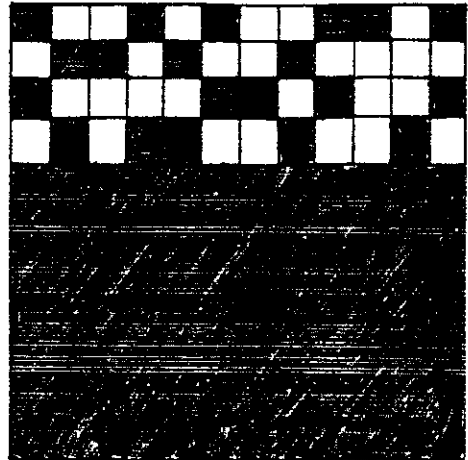


-3-

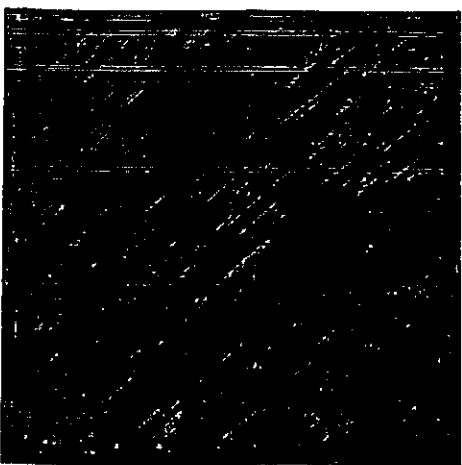
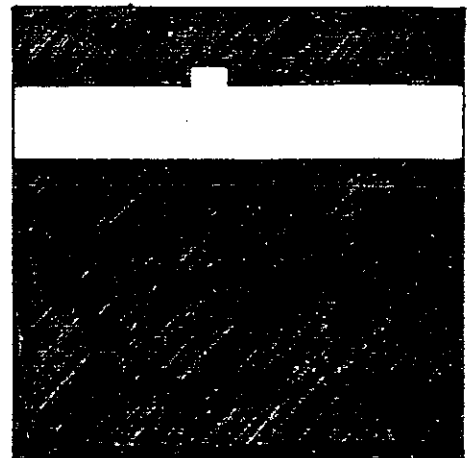




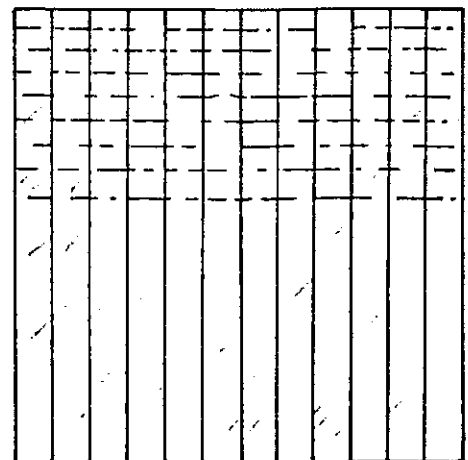
WR

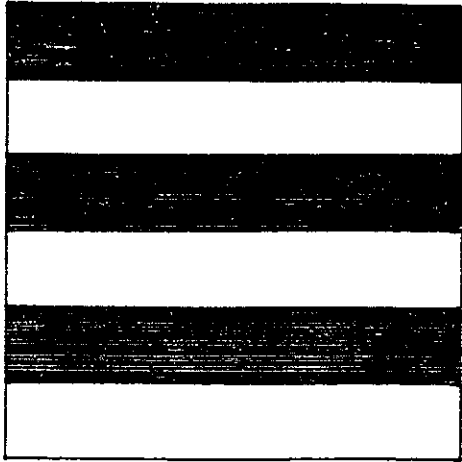


RAS

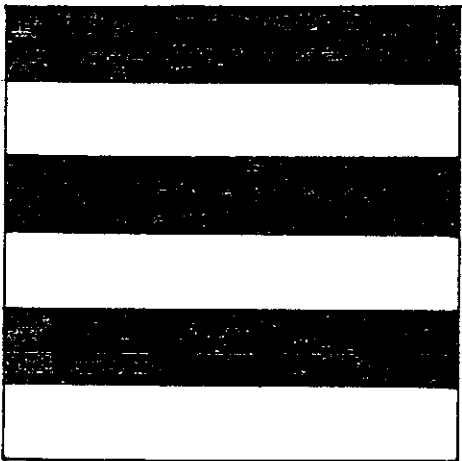
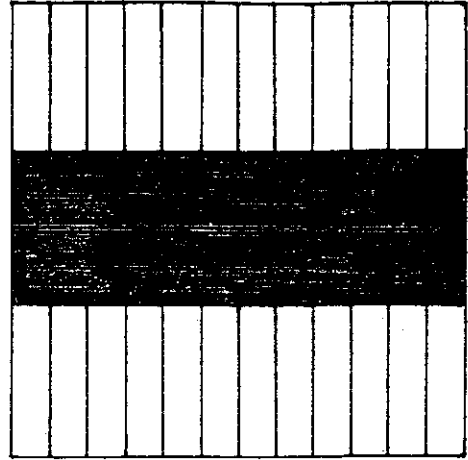


— MA7 —

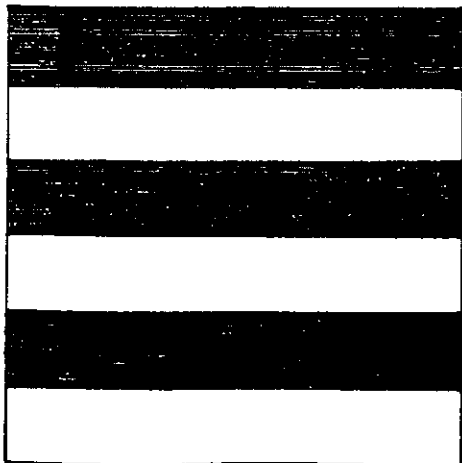
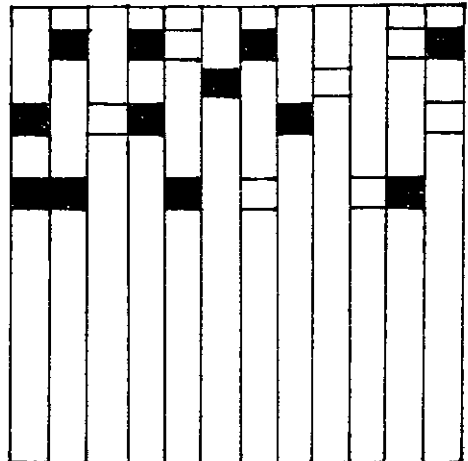




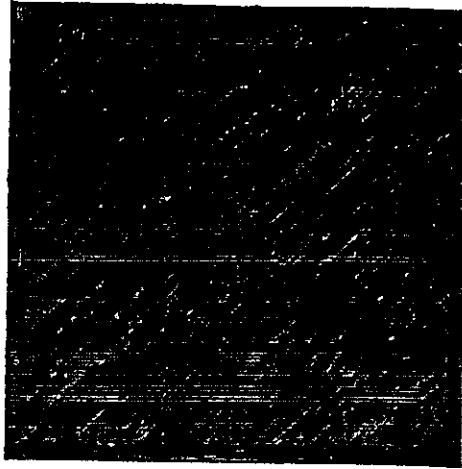
-MA 3-



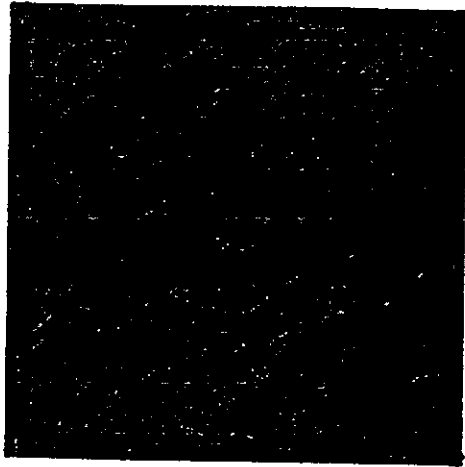
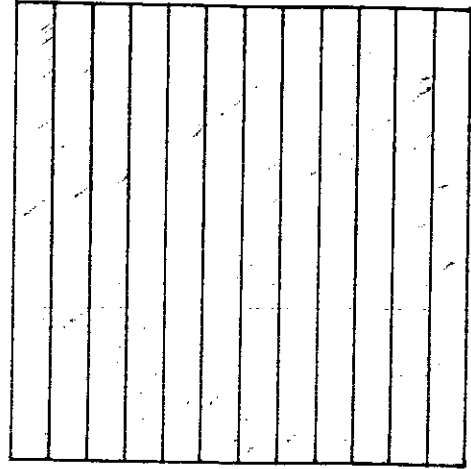
-MA 5-



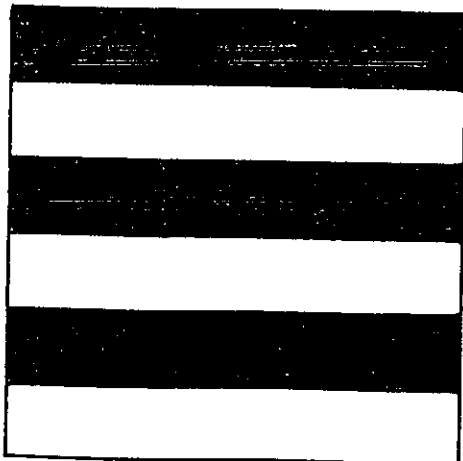
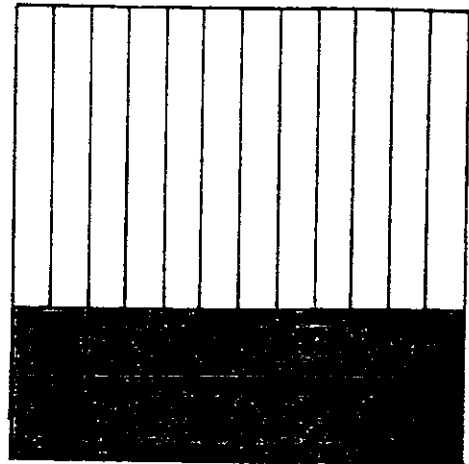
-MA 4, MA 6, CAS 1 , CAS 2



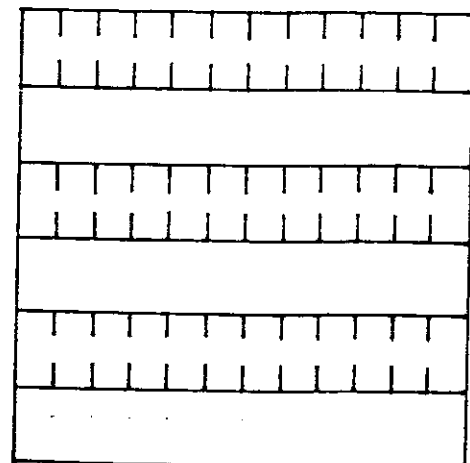
-MA 0-



-MA 1-

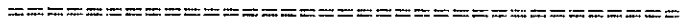


-MA 2-

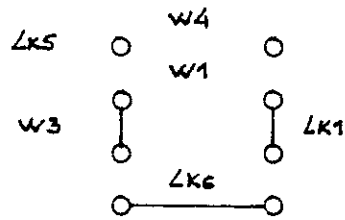


As figuras descritas determinam o modo de posicionamento dos Jumper's para os diversos tipos (Fabricantes) de Rom a serem utilizados no TC 2048.

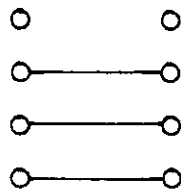
JUMPER TC 2048 (Issue 4)



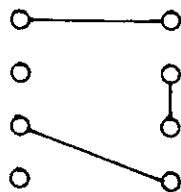
ROM HITACHI -GI- -AMI-



ROM NEC

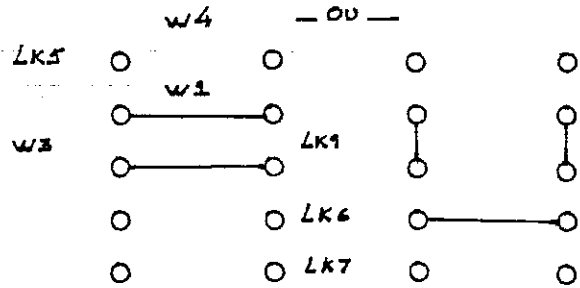


ROM - EPROM-

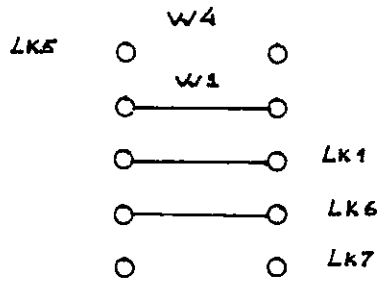


JUMPER TO 2048 (Issue 5)

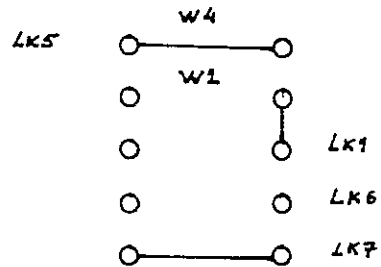
ROM HITACHI -GI- -AMI-



ROM NEC



ROM - EPROM-



TESTE FINAL COM " EPROM DE TESTE "

=====

1 - OBJECTIVO:

Testar a Funcionalidade do Computador TC 2048

2 - EQUIPAMENTO NECESSARIO:

- Interface com EPROM de Teste (TE 9410/03)
- Televisor a Cores (Deve estar de acordo com o tipo de codificação de cor e frequência da portadora utilizada no computador)
- Monitor monocromático
- Fonte de Alimentação TC2048
- Joystick
- Cassette do programa " Load OK " (TE-9300/01/xx)
- Gravador
- Vuímetro (Fig.1) ou Circuito Detector (Fig.2)

3 - METODO DE TESTE:

- Introduzir o Interface no EDGE CONNECTOR do computador
- Ligar o cabo de "TV" e "Monitor" aos respectivos aparelhos
- Ligar a Fonte de Alimentação

4 - SINAIS DE CONTROLE E ESCRITA NO Edge Connector:

- Após ter-se ligado o computador (Power ON), e caso não existirem sinais de escrita, aparece no ecran a seguinte mensagem : " Verifique os sinais de control de escrita no EDGE CONNECTOR ".
Caso contrário, não aparece nenhuma mensagem no ecran e passa ao teste seguinte.

5 - TESTE DE COR:

Aparece no ecran um conjunto de riscas coloridas em duas tonalidades de brilho.

Deve responder à questão posta pressionando na tecla " S " para continuar.

6 - TESTE DE SAVE:

Observe um conjunto de riscas de cor "Azul" e "Vermelha" deslizando no sentido horizontal de baixo para cima do ecran. Verifique se o indicador de nível atinge o valor correcto ou o led do circuito detector permanece aceso durante o

7 - TESTE DE SOM:

São gerados um conjunto de notas musicais distintas umas das outras.

Não deve existir distorção no som.

Para repetir o teste, pressione a tecla "R".

Para prosseguir o teste, pressione a tecla "S".

8 - TESTE DO TECLADO:

Surgirá no ecran, um conjunto de caracteres representando o código de cada tecla, pertencente ao teclado. Deverá apagá-los tendo para isso de pressionar a tecla correspondente, começando pela tecla "1" e depois sequencialmente.

9 - TESTE DE RAM E ROM:

Aparece no televisor uma sucessão de ecrans com cores aleatórias, num determinado espaço de tempo, aparecendo no fim a mensagem: " Este TC2048 tem 48K de memória "

" Rom OK "

Caso o computador tenha anomalias no banco de memória ou na Rom, aparece a seguinte mensagem: " Falha na Ram "; "Rom falhou".

10- TESTE DO SCLD:

Aparece durante alguns segundos na zona do border, uma sequência de pequenas riscas pretas acompanhadas de som. Após este período de tempo, a mensagem indicativa de "teste do SCLD" toma diversos formatos.

A mensagem que deve aparecer no ecran no fim do teste é: " SCLD OK ".

11- TESTE DO JOYSTICK:

Deve surgir no ecran a seguinte mensagem:

CIMA
ESQUERDA DIREITA
BAIXO

Com o Joystick inserido na respectiva ficha, deve aceder a cada uma das instruções.

12- TESTE DO LOAD:

Ligue o cabo do gravador ao Jack EAR do computador, e pressione a tecla PLAY do gravador.

Após o programa estar carregado, surge no ecran a mensagem "LOAD OK".

Se o computador passar a todos testes atrás descritos, então encontra-se " APROVADO ".

Deve desligar primeiro a alimentação, e depois todos outros periféricos.

Fig. 1

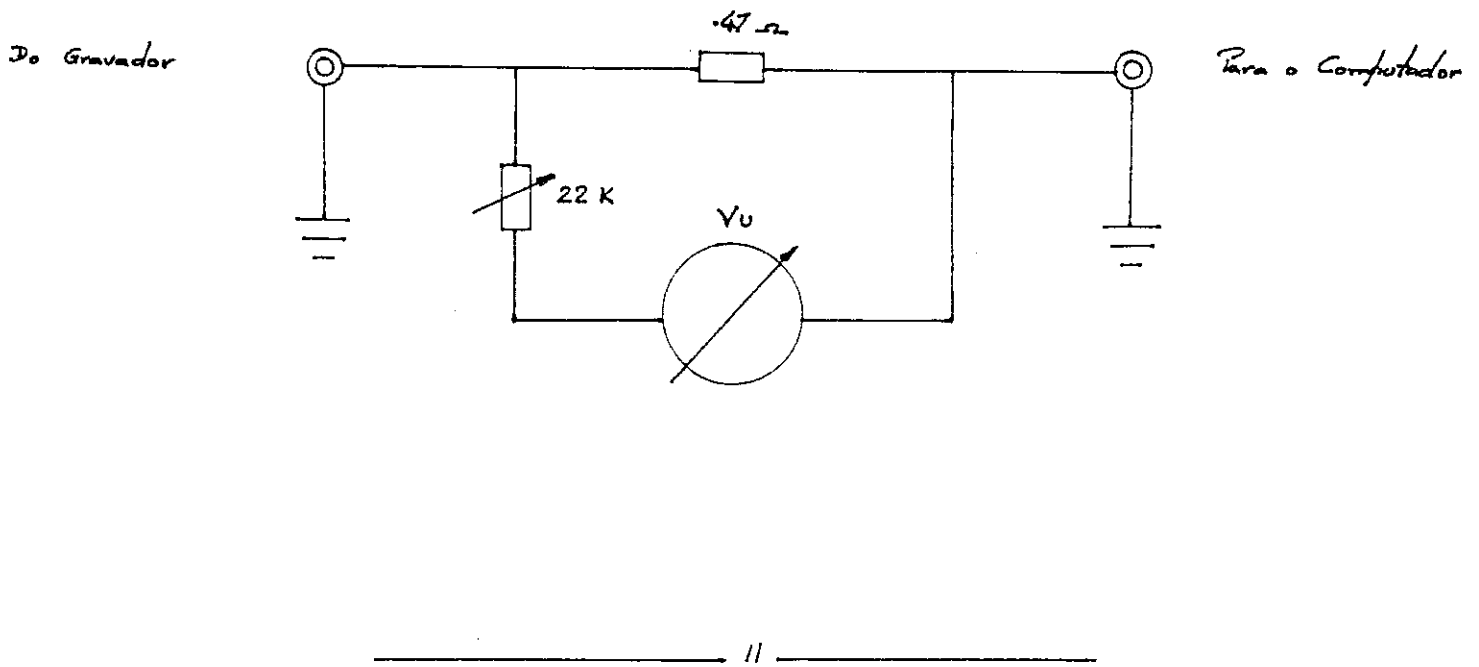
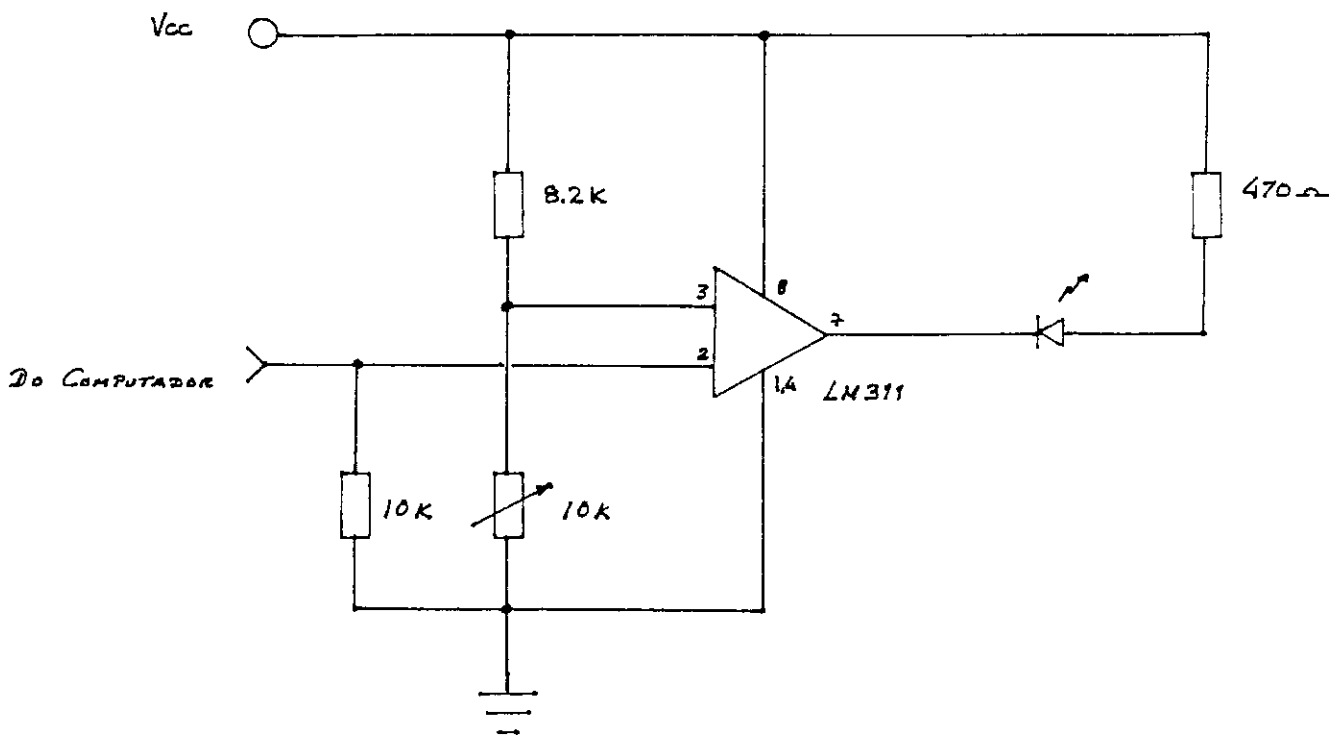
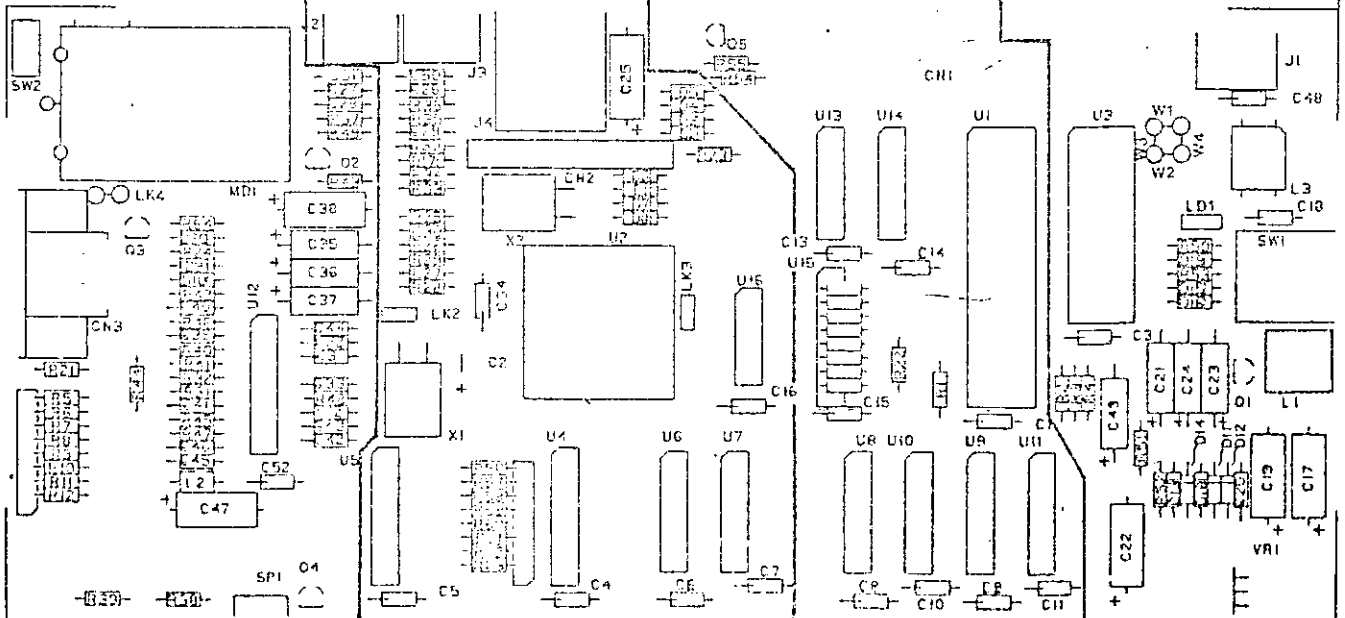


Fig. 2



IC	U12	U2. U4. U5. U6. U7. U16.	U1. U14. U8. U15. U9. U10. U11. U13.	U3. VR1.
R	5. 12. 39. 47. 6. 21. 40. 48. 7. 24. 41. 49. 8. 31. 43. 9. 32. 44. 10. 37. 45. 11. 38. 46.	23. 33. 59. 25. 34. 60. 26. 35. 61. 27. 36. 62. 28. 56. 63. 29. 57. 30. 58.	1. 22. 53. 55.	2. 3. 4. 50. 51. 52. 53.
C	12. 36. 43. 27. 37. 44. 28. 38. 45. 31. 39. 46. 32. 40. 47. 33. 41. 51. 35. 42. 52.	2. 26. 4. 29. 5. 30. 6. 34. 7. 50. 10. 25.	1. 8. 9. 10. 11. 13. 14.	3. 23. 17. 24. 18. 48. 19. 49. 20. 21. 22.
D	D9. D10. D20.	1. 8. 2. 17. 3. 4. 5. 6. 7.		11. 15. 12. 16. 13. 14. 18. 19.
TR	Q2. Q3. Q4		Q5.	Q1.
MISC.	Modulador (MD1) Ficha 9 pin Joyst. (CN3) Check (L2) Loadspeaker	J2 (MIC) X1 (4.433619) J3 (EAR) X2 (14.000) J4 (Video) CN2 (teclado)	CN1 (Edge Connector)	J1 (Alimentação) L3 (Check) L1 (transformador DC/DC) SW1 (Interruptor ON/OFF) LD1 (LED)



Parts List TC2048 Issue 02

Resistências						
Res.	100R	:	1/4W	:	+/-5%	CF * R45, 51
Res.	220R	:	1/4W	:	+/-5%	CF * R54
Res.	270R	:	1/4W	:	+/-5%	CF * R36, 44
Res.	470R	:	1/4W	:	+/-5%	CF * R13-20, R28-30
Res.	680R	:	1/4W	:	+/-5%	CF * R23, 35, 37, 50
Res.	1K	:	1/4W	:	+/-5%	CF * R3, 31, 32, 65
Res.	1K5	:	1/4W	:	+/-5%	CF * R2
Res.	2K2	:	1/4W	:	+/-5%	CF * R22, 47, 52, 53
Res.	4K7	:	1/4W	:	+/-5%	CF * R25, 27, 55
Res.	5K1	:	1/4W	:	+/-5%	CF * R26
Res.	6K8	:	1/4W	:	+/-5%	CF * R33
Res.	10K	:	1/4W	:	+/-5%	CF * R1, R5-12, 21, 38, 40, R56-63
Res.	33K	:	1/4W	:	+/-5%	CF * R24, 42
Res.	47K	:	1/4W	:	+/-5%	CF * R46
Res.	62K	:	1/4W	:	+/-5%	CF * R41
Res.	100K	:	1/4W	:	+/-5%	CF * R39
Res.	220K	:	1/4W	:	+/-5%	CF * R4

Parts List TC2048 Issue 02

===== Condensadores =====			
Cap.	16Pf:50V:+/-5%:Cer.	Ax.	* C33
Cap.	47Pf:50V:+/-5%:Cer.	Ax.	* C34,45
Cap.	220Pf:50V:+80%-20%:Cer.	Ax.	* C31,32
Cap.	1Nf:50V:+80%-20%:Cer.	Ax.	* C26
Cap.	10Nf:50V:+80%-20%:Cer.	Ax.	* C29,41,44,46
Cap.	47Nf:50V:+80%-20%:Cer.	Ax.	* C18,27,48
Cap.	100Nf:50V:+80%-20%:Cer.	Ax.	* C1,3-14,16,20,28,30,39,42 C42,52 C22,47,52,53
Cap.	1Uf:16V:+50%-10%:El.	Ax.	* C23,24,49
Cap.	4.7Uf:25V:+50%-10%:El.	Ax.	* C53
Cap.	22Uf:16V:+50%-10%:El.	Ax.	* C19,21,35,37
Cap.	100Uf:16V:+75%-10%:El.	Ax.	* C17,22,38,47
Cap.	100Uf:10V:+75%-10%:El.	Ax.	* C25

Parts List TC204B Issue 02

=====
Diodos
=====

Diodo: 1N4001 (1.0A)	*	D11,12,14
Diodo: 1N4148	*	D1-10,13,15,16,17,20,21
Diodo Zenner: 12V	*	D18
Diodo Zenner: 5V1	*	D19

=====
Transistores
=====

Transistor, 2N 2222	*	Q2,6
Transistor, ZTX 750	*	Q1
Transistor, ZTX 313	*	Q3,5
Transistor, ZTX 450	*	Q4

Parts List TC2048 Issue 02

=====
Circuitos Integrados
=====

IC, Z80A (CPU)	*	U1
IC, MC1377N	*	U12
IC, 74LS157	*	U13,14
IC, D23128C (ROM)	*	U3
IC, 7805 Volt. Reg. (+5V)	*	VR1
IC, 4416-15NL Mos Dynamic Ram	*	U6-11
IC, 74LS245	*	U4
IC, 74LS244	*	U5
IC, 74LS92	*	U16

=====
Cristais
=====

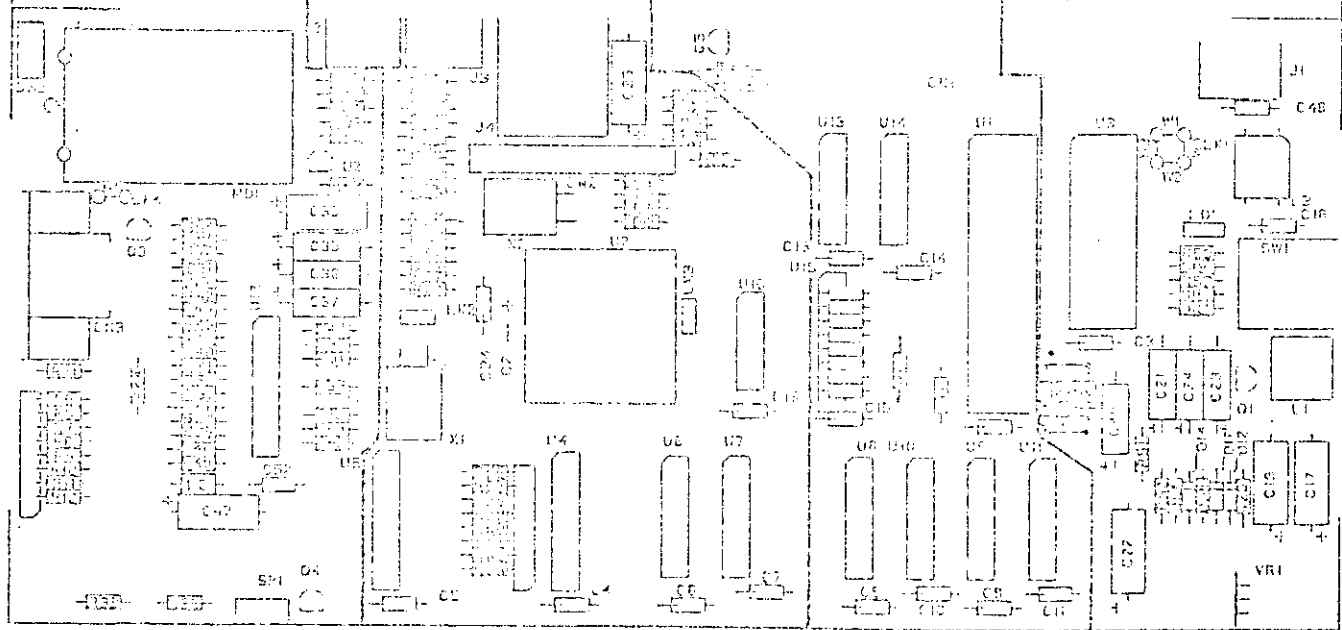
Cristal, 14MHZ Metal Type	*	X2
Cristal, 4.43519 MHZ Metal Type*		X1

=====
Miscellaneous
=====

Jack, Right Angle RCA VIDEO	*	J4
LED, Red P40 (Sanyo)	*	LD1
Modulador, UHF Tayud/EU 36 UHF Astec/UM 1233F36	*	MD1
Socket, Dll 40 ways (Single Contact	*	U1
Socket, Dll 28 ways (Single Contact	*	U3
Conn, Flex Cable 14 ways (Female)	*	CN2
Conn, Joystick 9 Pin (Male)	*	CN3
Socket Power, +9V	*	J1
Jack, Mini Phone (MIC/EAR)	*	J2,3
Transformador DC/DC	*	L1
Coil: 22UH : +/-5% : Ax.	*	L2

IC	U12.	U2. U4. U6. U7. U16. U5.	U1. U3. U8. U9. U10. U11. U13. U14.	U3 VR1.
R	5. 17. 39. 47. 6. 21. 40. 48. 7. 24. 42. 49. 8. 31. 45. 42. 9. 37. 44. 10. 37. 45. 11. 30. 45.	23. 34. 59. 25. 30. 60. 26. 35. 61. 27. 36. 62. 28. 36. 63. 29. 57. 30. 58.	1. 54. 55.	2. 3. 4. 50. 51. 52. 53.
C	12. 36. 43. 27. 37. 46. 28. 36. 45. 31. 39. 46. 32. 40. 47. 33. 41. 51. 35. 42. 52.	2. 26. 4. 29. 5. 38. 6. 34. 7. 50.	14. 15. 8. 9. 10. 11. 13. 17.	3. 13. 17. 24. 18. 48. 19. 49. 20. 21. 22.
D	U9. U10. U20.	1. 7. 2. 8. 3. 17. 4. 5. 6.		11. 16. 12. 17. 13. 20. # 14. 15. 16.
TR	Q2. Q3. Q4.		Q5	Q1

Misc.	Modulador (MB1) Ficha 9 pines Javat. (CP2) Clock (L2) Localizador	J2 (TFF) X1 (4.403619) J3 (L1) J4 (Vidéo) X2 (14 000) CIP (relé 120)	CR1 (Edge Converter)	J1 (Alimentação) V3 (Clock) L1 (Super Forwarder DC/DC) SP1 (Interruptor ON/OFF) D01 (L17)
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FACE COMPONENTES 206-950100-03-04

Parts List TC2048 Issue 03/04

Resistências

Res,	15R:	1/4W: +/-5%:	CF	*	R43,48
Res,	75R:	1/4W: +/-5%:	CF	*	R49
Res,	100R:	1/4W: +/-5%:	CF	*	R45,51
Res,	220R:	1/4W: +/-5%:	CF	*	R54
Res,	270R:	1/4W: +/-5%:	CF	*	R44
Res,	470R:	1/4W: +/-5%:	CF	*	R13-20, R28-30
Res,	680R:	1/4W: +/-5%:	CF	*	R20, 37, 50
Res,	1K:	1/4W: +/-5%:	CF	*	R3, 31, 32, 36
Res,	1K5:	1/4W: +/-5%:	CF	*	R2
Res,	2K2:	1/4W: +/-5%:	CF	*	R47, 53
Res,	4K7:	1/4W: +/-5%:	CF	*	R25, 27, 52, 55
Res,	5K1:	1/4W: +/-5%:	CF	*	R26
Res,	6KB:	1/4W: +/-5%:	CF	*	R35
Res,	10K:	1/4W: +/-5%:	CF	*	R1, R5-12, 21, 38, 40, 56, 63
Res,	33K:	1/4W: +/-5%:	CF	*	R24, 42
Res,	47K:	1/4W: +/-5%:	CF	*	R46
Res,	62K:	1/4W: +/-5%:	CF	*	R34, 41
Res,	100K:	1/4W: +/-5%:	CF	*	R39
Res,	220K:	1/4W: +/-5%:	CF	*	R4
Res,	390K:	1/4W: +/-5%:	CF	*	R33

Parts List TD204B Issue 03/04

=====
 Condensadores
 =====

Cap,	16Pf:50V:+/-5%:	Der.Ax	*	C33
Cap,	47Pf:50V:+/-5%:	Der.Ax	*	C34
Cap,	220Pf:50V:+80-20%:	Der.Ax	*	C31,32
Cap,	1Nf:50V:+80-20%:	Der.Ax	*	C26,29
Cap,	10Nf:50V:+80-20%:	Der.Ax	*	C41,44,46
Cap,	47Nf:50V:+80-20%:	Der.Ax	*	C18,27,48
Cap,	100Nf:50V:+80-20%:	Der.Ax	*	D1,C3-14,16,20,28,30,38,42, C43,52
Cap,	10uf:50V:+75-10%:	El.Ax	*	C23,24,49
Cap,	220uf:16V:+50-10%:	El.Ax	*	C19,21,35-37
Cap,	1000uf:16V:+75-10%:	El.Ax	*	C17,22,25,38,47

=====
 Diodos
 =====

Diodo,	1N 4148	*	D1-10,13,15,16
Diodo,	1N 4148	*	R4-Assemblado em Paralelo-
Diodo,	1N 4001 (1.A)	*	D11,12,14
Diodo Zener,	12V	*	D16
Diodo Zener,	5.1V	*	D17,19

Parts List TC204B Issue 03/04

Transistores

Transistor, 2N 2222	*	Q2,6
Transistor, ZTX 750	*	Q1
Transistor, ZTX 313	*	Q3,5
Transistor, ZTX 450	*	Q4

Circuitos Integrados

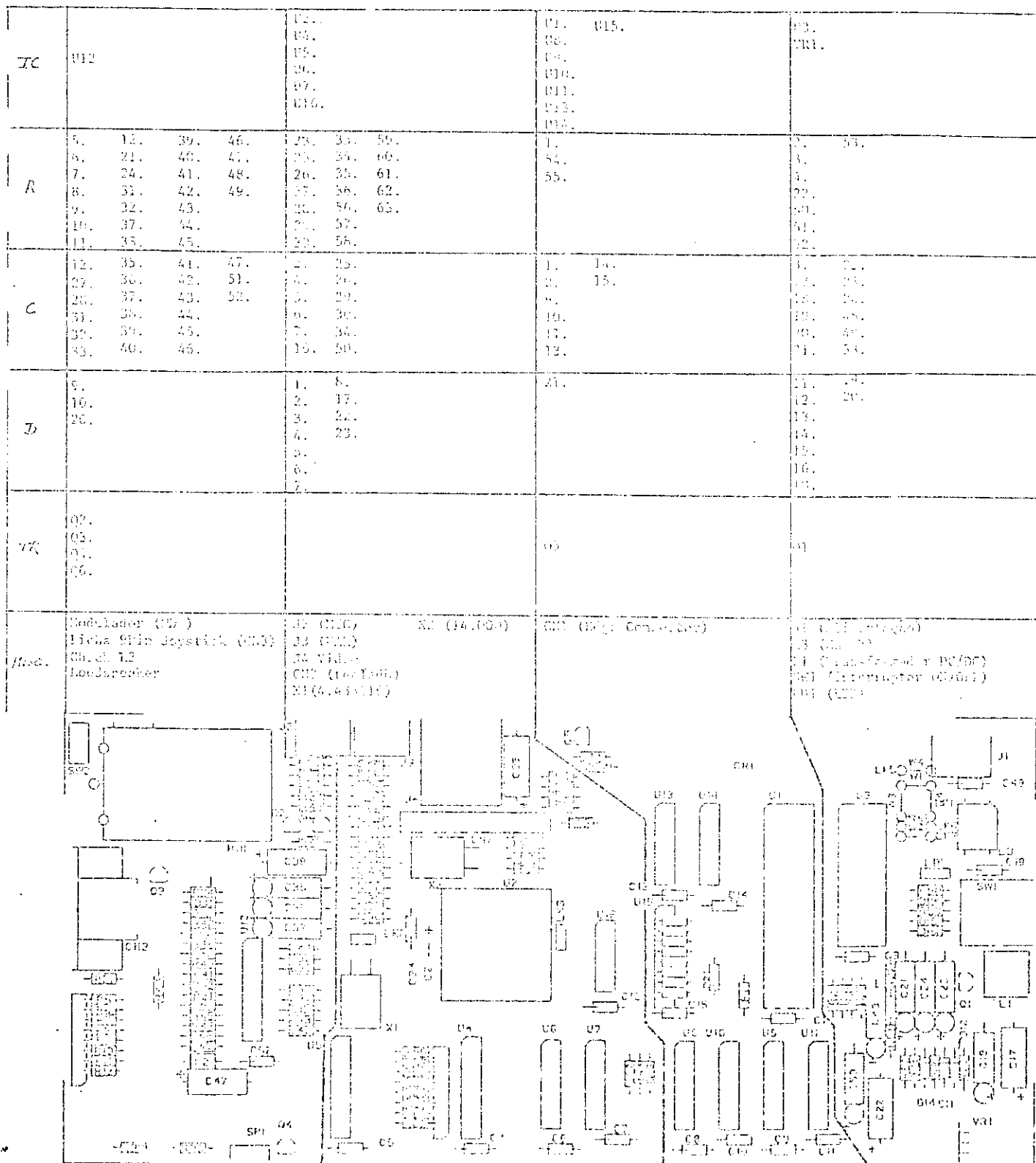
IC, Z80A (CPU)	*	U1
IC, MC 1377N	*	U12
IC, 74LS157	*	U13,14
IC, D23128C (ROM)	*	U3
IC, 7805 Volt.Reg. (+5V)	*	VR1
IC, 4416-15NL MOS Dynamic Ram	*	U6,7
IC, 4416-20NL MOS Dynamic Ram	*	U8-11
IC, 74LS245	*	U4
IC, 74LS244	*	U5
IC, 74LS32	*	U16

Cristais

Cristal, 14 MHZ Metal Type	*	X2
Cristal, 4.43619 MHZ Metal Type	*	X1

Parts List TC2048 Issue 03/04

Miscellaneous		
Jack, Right Angle RCA Video	*	J4
Jack, Mini Phone (EAR,MIC)	*	J2,3
Socket, Dll 40 Ways (Single Contact)	*	U1
Socket, Dll 28 Ways (Single Contact)	*	U3
Conn, Joystick 9 Pin (Male)	*	CN3
Conn, Flex Cable 14 Ways (Female)	*	CN2
Socket, Power 9 Volts	*	J1
Transformador, DC/DC	*	L1
Coil, 22UH : +/-5% : Ax	*	L2



Parts List TC2048 Issue 05

Resistências		
Res, 15R: 1/4W: +/-5%: CF	*	R43, 48
Res, 75R: 1/4W: +/-5%: CF	*	R49
Res, 100R: 1/4W: +/-5%: CF	*	R45, 51
Res, 220R: 1/4W: +/-5%: CF	*	R54
Res, 270R: 1/4W: +/-5%: CF	*	R44
Res, 470R: 1/4W: +/-5%: CF	*	R13-20, R28-30
Res, 680R: 1/4W: +/-5%: CF	*	R23, 37, 50
Res, 1K: 1/4W: +/-5%: CF	*	R3, 31, 32, 36
Res, 1k5: 1/4W: +/-5%: CF	*	R2
Res, 2k2: 1/4W: +/-5%: CF	*	R47, 53
Res, 4k7: 1/4W: +/-5%: CF	*	R25, 27, 52, 55
Res, 5k1: 1/4W: +/-5%: CF	*	R26
Res, 6k8: 1/4W: +/-5%: CF	*	R35
Res, 10K: 1/4W: +/-5%: CF	*	R1, 5-12, 21, 38, 40, 56-63
Res, 33K: 1/4W: +/-5%: CF	*	R24, 42
Res, 47K: 1/4W: +/-5%: CF	*	R46
Res, 62K: 1/4W: +/-5%: CF	*	R34, 41
Res, 100K: 1/4W: +/-5%: CF	*	R39
Res, 220K: 1/4W: +/-5%: CF	*	R4
Res, 390K: 1/4W: +/-5%: CF	*	R33

Parts List TC2048 Issue 05

=====
 Condensadores
 =====

Cap, 16Pf: 50V: +/-5%:Cer.Ax	*	C33
Cap, 47Pf: 50V: +/-5%:Cer.Ax	*	C34
Cap, 220Pf: 50V: +80%-20%:Cer.Ax	*	C31,32
Cap, 1nf: 50V: +80%-20%:Cer.Ax	*	C26,29
Cap, 10nf: 50V: +80%-20%:Cer.Ax	*	C41,44,46
Cap, 47Nf: 50V: +80%-20%:Cer.Ax	*	C18,27,48
Cap, 100nf: 50V: +80%-20%:Cer.Ax	*	C1,3-14,16,20,28,30,39
	*	42,43,52
Cap, 1uf: 50V: +75%-10%:El.Ax	*	C23,24,49
Cap, 22Uf: 16V: +50%-10%:El.Ax	*	C19,21,35-37
Cap, 100Uf: 16V: +75%-10%:El.Ax	*	C17,22,25,36,47

=====
 Diodos
 =====

Diodo, 1N 4148	*	D1-10,13,15,16,20
Diodo Zenner, 12V	*	D16
Diodo Zenner, 5V1	*	D17,19
Diodo, 1N 4001 (1.0A)	*	D11,12,14

Parts List TC2048 Issue 05

Transistores

Transistor, 2N 2222	*	Q2,6
Transistor, ZTX 750	*	Q1
Transistor, ZTX 313	*	Q3,5
Transistor, ZTX 450	*	Q4

Circuitos Integrados

IC, Z80A (CPU)	*	U1
IC, MC 1877N	*	U12
IC, 74LS157	*	U13,14
IC, Eeprom 27128 (V1.1)	*	U3
IC, 7805 Volt.Reg. (+5)	*	VR1
IC, 4416-15NL Mos Dynamic Ram	*	U6,7
IC, 41464C (41254C) Mos Dyna. Ram	*	U8,9
IC, 74LS245	*	U4
IC, 74LS244	*	U5
IC, 74LS32	*	U16

Cristais

Cristal, 14MHZ Metal Type	*	X2
Cristal, 4.43619MHZ Metal Type	*	X1

Parts List TC2048 Issue 05

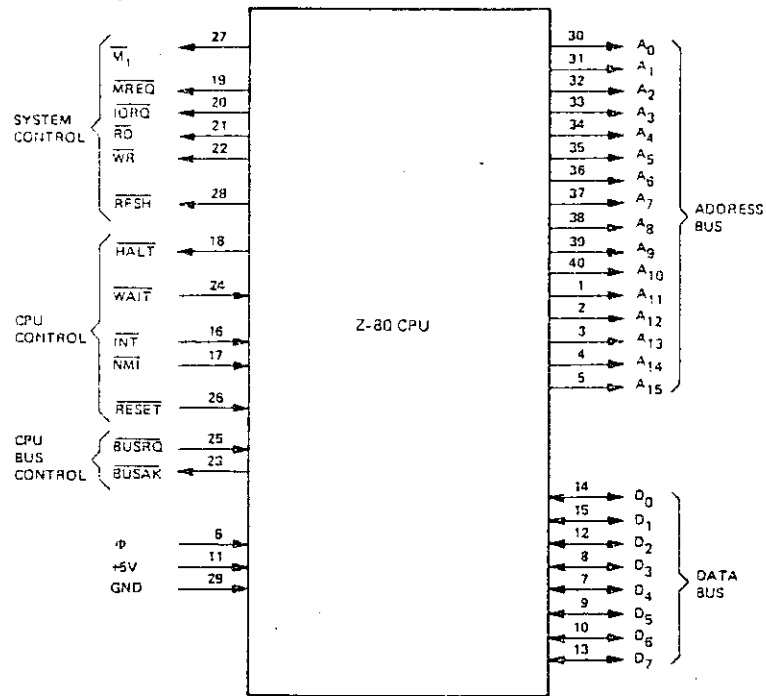
Miscellaneous

Jack, Right Angle RCA Video	*	J4
Jack, Mini Phone (Ear, Mic)	*	J2,3
Socket, Dll 40 Ways (Single Contact)	*	U1
Socket, Dll 28 Ways (Single Contact)	*	U3
Conn. Joystick 9 Pin (Male)	*	CN3
Conn. Flex Cable 14 Ways (Female)	*	CN2
Socket, Power 9 Volts	*	J1
Transformador, DC/DC	*	L1
Coil, 22UH : +/-5% : Ax	*	L2

Especificações Técnicas do CPU I-80 IC1

3.0 Z-80 CPU PIN DESCRIPTION

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in figure 3.0-1 and the function of each is described below.



Z-80 PIN CONFIGURATION
FIGURE 3.0-1

A_0-A_{15}
(Address Bus)

Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D_0-D_7
(Data Bus)

Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

\overline{M}_1
(Machine Cycle one)

Output, active low. \overline{M}_1 indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, \overline{M}_1 is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. \overline{M}_1 also occurs with \overline{IORQ} to indicate an interrupt acknowledge cycle.

\overline{MREQ}
(Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{\text{IORQ}}$ (Input/Output Request)	Tri-state output, active low. The $\overline{\text{IORQ}}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{\text{IORQ}}$ signal is also generated with an $\overline{\text{MI}}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M_1 time while I/O operations never occur during M_1 time.
$\overline{\text{RD}}$ (Memory Read)	Tri-state output, active low. $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{\text{WR}}$ (Memory Write)	Tri-state output, active low. $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
$\overline{\text{RFSH}}$ (Refresh)	Output, active low. $\overline{\text{RFSH}}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{\text{MREQ}}$ signal should be used to do a refresh read to all dynamic memories.
$\overline{\text{HALT}}$ (Halt state)	Output, active low. $\overline{\text{HALT}}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.
$\overline{\text{WAIT}}$ (Wait)	Input, active low. $\overline{\text{WAIT}}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.
$\overline{\text{INT}}$ (Interrupt Request)	Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{\text{BUSRQ}}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{\text{IORQ}}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).
$\overline{\text{NMI}}$ (Non Maskable Interrupt)	Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{\text{NMI}}$ automatically forces the Z-80 CPU to restart to location 0060H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous $\overline{\text{WAIT}}$ cycles can prevent the current instruction from ending, and that a $\overline{\text{BUSRQ}}$ will override a $\overline{\text{NMI}}$.

RESET

Input, active low. RESET forces the program counter to zero and initializes the CPU. The CPU initialization includes:

- 1) Disable the interrupt enable flip-flop
- 2) Set Register I = 00₁₁
- 3) Set Register R = 00₁₁
- 4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state.

BUSRQ
(Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.

BUSAK
(Bus Acknowledge)

Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

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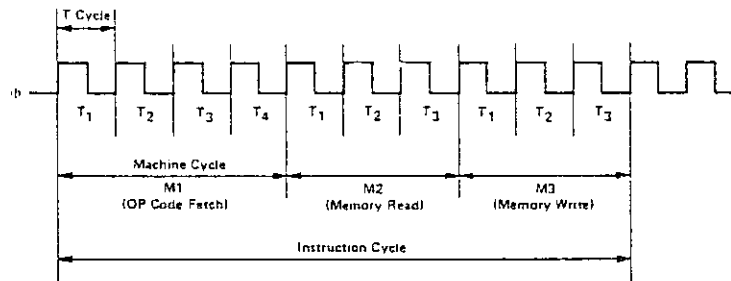
Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

4.0 CPU TIMING

The Z-80 CPU executes instructions by stepping through a very precise set of a few basic operations. These include:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

All instructions are merely a series of these basic operations. Each of these basic operations can take from three to six clock periods to complete or they can be lengthened to synchronize the CPU to the speed of external devices. The basic clock periods are referred to as T cycles and the basic operations are referred to as M (for machine) cycles. Figure 4.0-0 illustrates how a typical instruction will be merely a series of specific M and T cycles. Notice that this instruction consists of three machine cycles (M1, M2 and M3). The first machine cycle of any instruction is a fetch cycle which is four, five or six T cycles long (unless lengthened by the wait signal which will be fully described in the next section). The fetch cycle (M1) is used to fetch the OP code of the next instruction to be executed. Subsequent machine cycles move data between the CPU and memory or I/O devices and they may have anywhere from three to five T cycles (again they may be lengthened by wait states to synchronize the external devices to the CPU). The following paragraphs describe the timing which occurs within any of the basic machine cycles. In section 7, the exact timing for each instruction is specified.



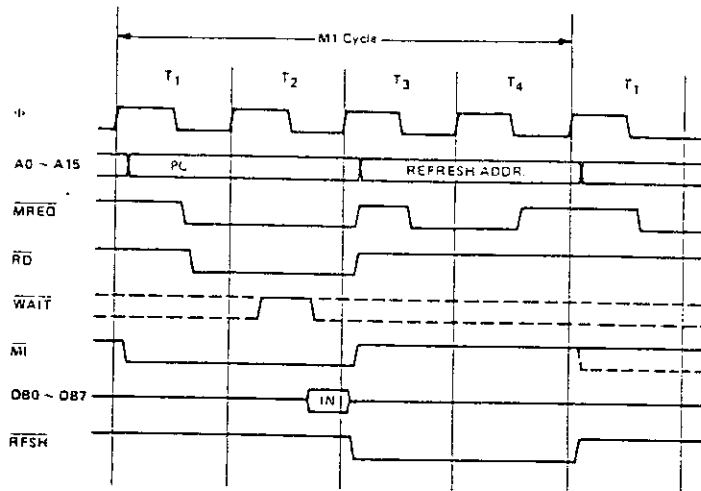
BASIC CPU TIMING EXAMPLE
FIGURE 4.0-0

All CPU timing can be broken down into a few very simple timing diagrams as shown in figure 4.0-1 through 4.0-7. These diagrams show the following basic operations with and without wait states (wait states are added to synchronize the CPU to slow memory or I/O devices).

- 4.0-1. Instruction OP code fetch (M1 cycle)
- 4.0-2. Memory data read or write cycles
- 4.0-3. I/O read or write cycles
- 4.0-4. Bus Request/Acknowledge Cycle
- 4.0-5. Interrupt Request/Acknowledge Cycle
- 4.0-6. Non maskable Interrupt Request/Acknowledge Cycle
- 4.0-7. Exit from a HALT instruction

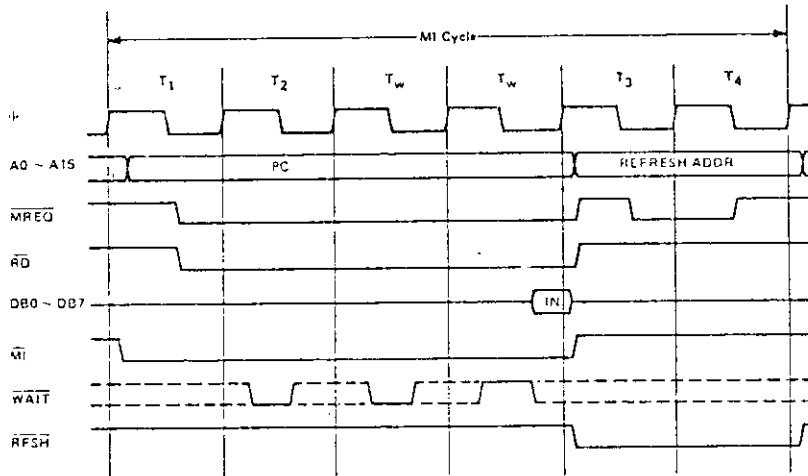
INSTRUCTION FETCH

Figure 4.0-1 shows the timing during an M1 cycle (OP code fetch). Notice that the PC is placed on the address bus at the beginning of the M1 cycle. One half clock time later the \overline{MREQ} signal goes active. At this time the address to the memory has had time to stabilize so that the falling edge of \overline{MREQ} can be used directly as a chip enable clock to dynamic memories. The \overline{RD} line also goes active to indicate that the memory read data should be enabled onto the CPU data bus. The CPU samples the data from the memory on the data bus with the rising edge of the clock of state T3 and this same edge is used by the CPU to turn off the \overline{RD} and \overline{MREQ} signals. Thus the data has already been sampled by the CPU before the \overline{RD} signal becomes inactive. Clock state T3 and T4 of a fetch cycle are used to refresh dynamic memories. (The CPU uses this time to decode and execute the fetched instruction so that no other operation could be performed at this time). During T3 and T4 the lower 7 bits of the address bus contain a memory refresh address and the \overline{RFSH} signal becomes active to indicate that a refresh read of all dynamic memories should be accomplished. Notice that a \overline{RD} signal is not generated during refresh time to prevent data from different memory segments from being gated onto the data bus. The \overline{MREQ} signal during refresh time should be used to perform a refresh read of all memory elements. The refresh signal can not be used by itself since the refresh address is only guaranteed to be stable during \overline{MREQ} time.



INSTRUCTION OP CODE FETCH
FIGURE 4.0-1

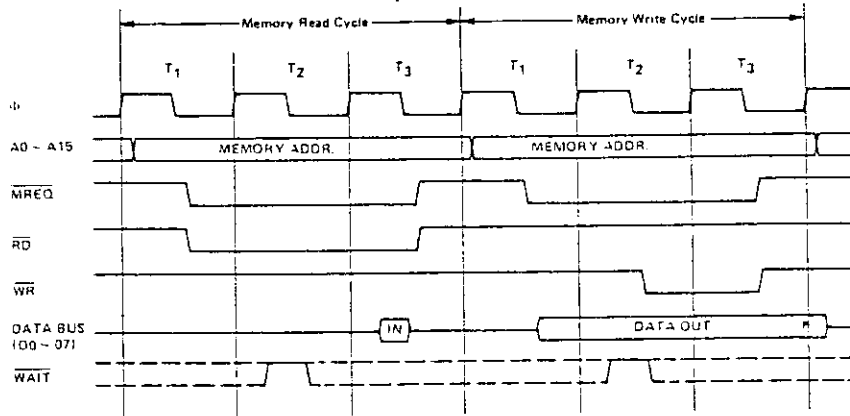
Figure 4.0-1A illustrates how the fetch cycle is delayed if the memory activates the \overline{WAIT} line. During T2 and every subsequent T_w , the CPU samples the \overline{WAIT} line with the falling edge of Φ . If the \overline{WAIT} line is active at this time, another wait state will be entered during the following cycle. Using this technique the read cycle can be lengthened to match the access time of any type of memory device.



INSTRUCTION OP CODE FETCH WITH WAIT STATES
FIGURE 4.0-1A

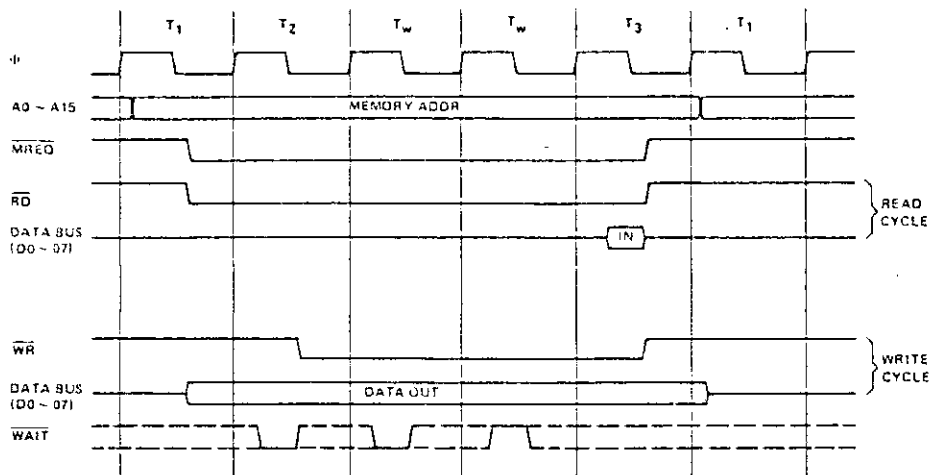
MEMORY READ OR WRITE

Figure 4.0-2 illustrates the timing of memory read or write cycles other than an OP code fetch (M1 cycle). These cycles are generally three clock periods long unless wait states are requested by the memory via the WAIT signal. The MREQ signal and the RD signal are used the same as in the fetch cycle. In the case of a memory write cycle, the MREQ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The WR line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory. Furthermore the WR signal goes inactive one half T state before the address and data bus contents are changed so that the overlap requirements for virtually any type of semiconductor memory type will be met.



MEMORY READ OR WRITE CYCLES
FIGURE 4.0-2

Figure 4.0-2A illustrates how a $\overline{\text{WAIT}}$ request signal will lengthen any memory read or write operation. This operation is identical to that previously described for a fetch cycle. Notice in this figure that a separate read and a separate write cycle are shown in the same figure although read and write cycles can never occur simultaneously.



MEMORY READ OR WRITE CYCLES WITH WAIT STATES
FIGURE 4.0-2A

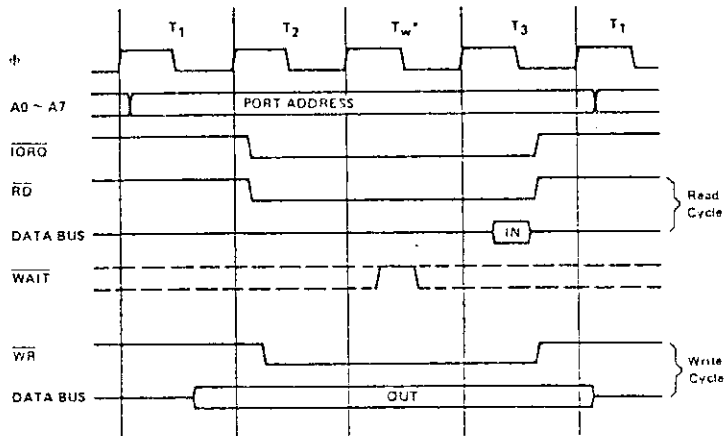
INPUT OR OUTPUT CYCLES

Figure 4.0-3 illustrates an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted. The reason for this is that during I/O operations, the time from when the IORQ signal goes active until the CPU must sample the $\overline{\text{WAIT}}$ line is very short and without this extra state sufficient time does not exist for an I/O port to decode its address and activate the $\overline{\text{WAIT}}$ line if a wait is required. Also, without this wait state it is difficult to design MOS I/O devices that can operate at full CPU speed. During this wait state time the $\overline{\text{WAIT}}$ request signal is sampled. During a read I/O operation, the RD line is used to enable the addressed port onto the data bus just as in the case of a memory read. For I/O write operations, the WR line is used as a clock to the I/O port, again with sufficient overlap timing automatically provided so that the rising edge may be used as a data clock.

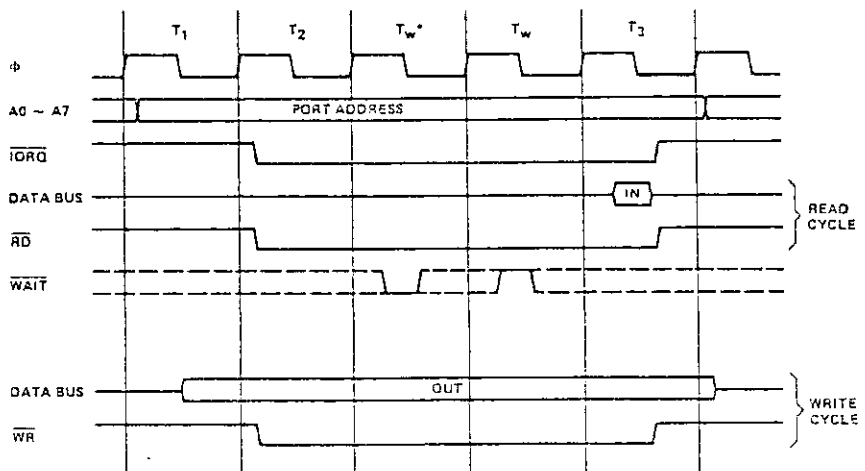
Figure 4.0-3A illustrates how additional wait states may be added with the $\overline{\text{WAIT}}$ line. The operation is identical to that previously described.

BUS REQUEST/ACKNOWLEDGE CYCLE

Figure 4.0-4 illustrates the timing for a Bus Request/Acknowledge cycle. The $\overline{\text{BUSRQ}}$ signal is sampled by the CPU with the rising edge of the last clock period of any machine cycle. If the $\overline{\text{BUSRQ}}$ signal is active, the CPU will set its address, data and tri-state control signals to the high impedance state with the rising edge of the next clock pulse. At that time any external device can control the buses to transfer data between memory and I/O devices. (This is generally known as Direct Memory Access [DMA] using cycle stealing). The maximum time for the CPU to respond to a bus request is the length of a machine cycle and the external controller can maintain control of the bus for as many clock cycles as is desired. Note, however, that if very long DMA cycles are used, and dynamic memories are being used, the external controller must also perform the refresh function. This situation only occurs if very large blocks of data are transferred under DMA control. Also note that during a bus request cycle, the CPU cannot be interrupted by either a NMI or an INT signal.

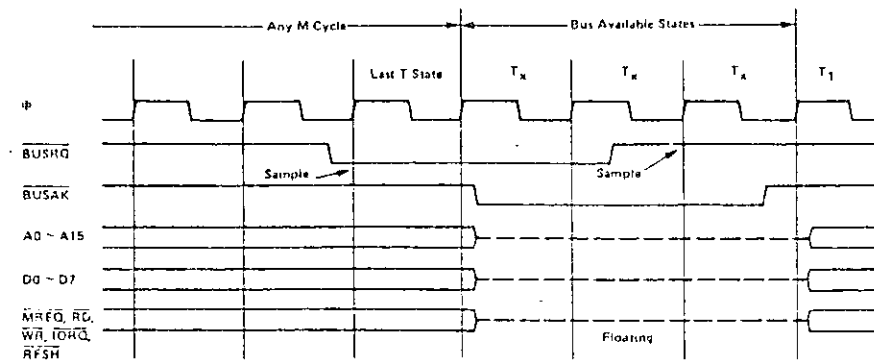


INPUT OR OUTPUT CYCLES
FIGURE 4.0-3



INPUT OR OUTPUT CYCLES WITH WAIT STATES
FIGURE 4.0-3A

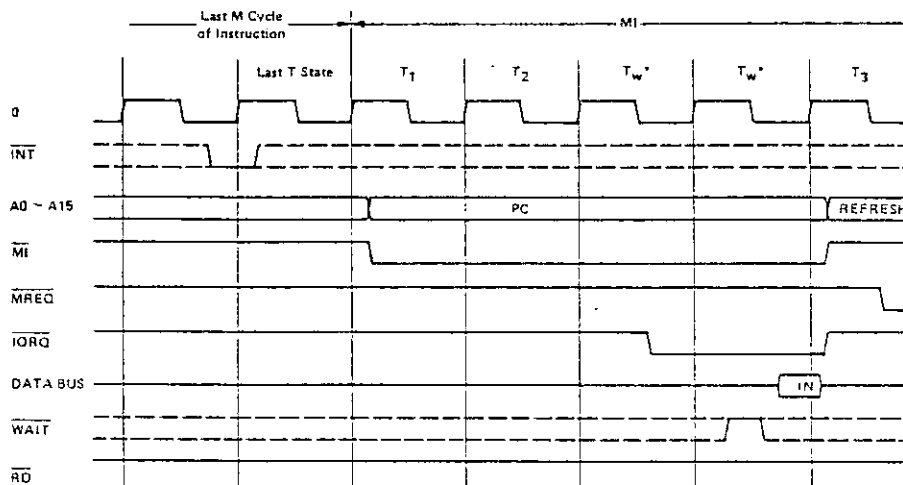
* Automatically inserted WAIT state



BUS REQUEST/ACKNOWLEDGE CYCLE
FIGURE 4.0-4

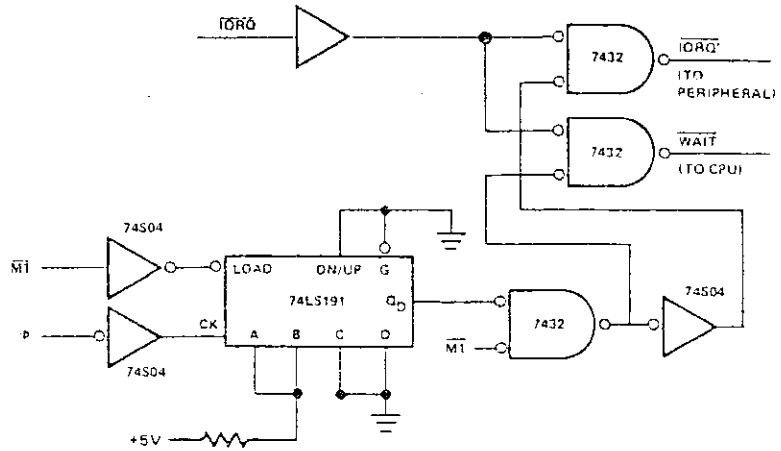
INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

Figure 4.0-5 illustrates the timing associated with an interrupt cycle. The interrupt signal (\overline{INT}) is sampled by the CPU with the rising edge of the last clock at the end of any instruction. The signal will not be accepted if the internal CPU software controlled interrupt enable flip-flop is not set or if the \overline{BUSRQ} signal is active. When the signal is accepted a special M1 cycle is generated. During this special M1 cycle the \overline{IORQ} signal becomes active (instead of the normal \overline{MREQ}) to indicate that the interrupting device can place an 8-bit vector on the data bus. Notice that two wait states are automatically added to this cycle. These states are added so that a ripple priority interrupt scheme can be easily implemented. The two wait states allow sufficient time for the ripple signals to stabilize and identify which I/O device must insert the response vector. Refer to section 8.0 for details on how the interrupt response vector is utilized by the CPU.

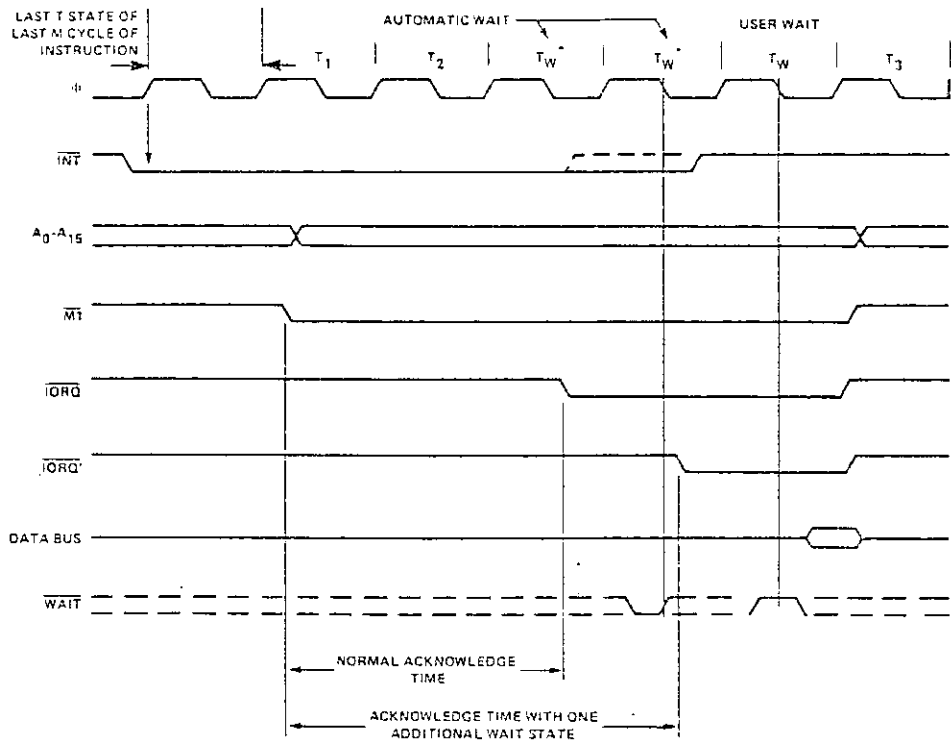


INTERRUPT REQUEST/ACKNOWLEDGE CYCLE
FIGURE 4.0-5

Figures 4.0-5A and 4.0-5B illustrate how a programmable counter can be used to extend interrupt acknowledge time. (Configured as shown to add one wait state)



EXTENDING INTERRUPT ACKNOWLEDGE TIME WITH WAIT STATE
FIGURE 4.0-5A



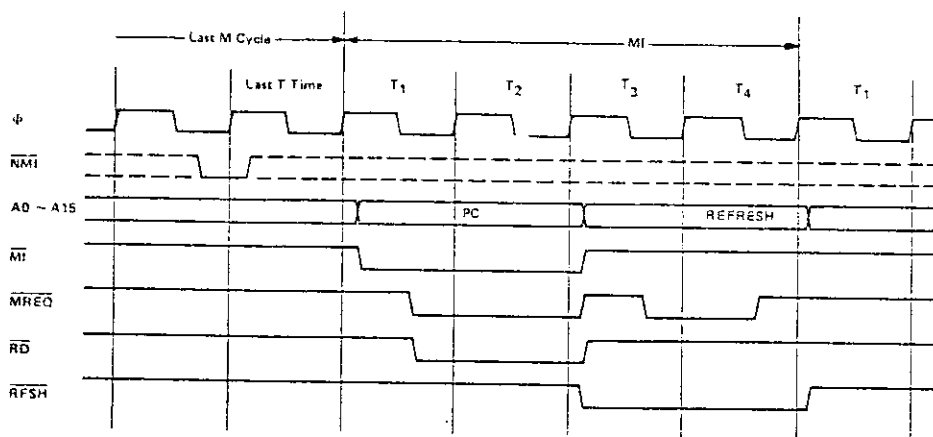
REQUEST/ACKNOWLEDGE CYCLE WITH ONE ADDITIONAL WAIT STATE
FIGURE 4.0-5B

NON MASKABLE INTERRUPT RESPONSE

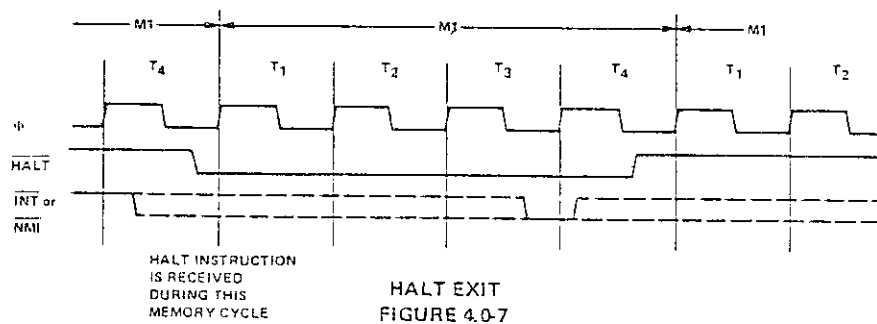
Figure 4.0-6 illustrates the request/acknowledge cycle for the non maskable interrupt. This signal is sampled at the same time as the interrupt line, but this line has priority over the normal interrupt and it can not be disabled under software control. Its usual function is to provide immediate response to important signals such as an impending power failure. The CPU response to a non maskable interrupt is similar to a normal memory read operation. The only difference being that the content of the data bus is ignored while the processor automatically stores the PC in the external stack and jumps to location 0066₁₁. The service routine for the non maskable interrupt must begin at this location if this interrupt is used.

HALT EXIT

Whenever a software halt instruction is executed the CPU begins executing NOP's until an interrupt is received (either a non maskable or a maskable interrupt while the interrupt flip flop is enabled). The two interrupt lines are sampled with the rising clock edge during each T4 state as shown in figure 4.0-7. If a non maskable interrupt has been received or a maskable interrupt has been received and the interrupt enable flip-flop is set, then the halt state will be exited on the next rising clock edge. The following cycle will then be an interrupt acknowledge cycle corresponding to the type of interrupt that was received. If both are received at this time, then the non maskable one will be acknowledged since it has highest priority. The purpose of executing NOP instructions while in the halt state is to keep the memory refresh signals active. Each cycle in the halt state is a normal M1 (fetch) cycle except that the data received from the memory is ignored and a NOP instruction is forced internally to the CPU. The halt acknowledge signal is active during this time to indicate that the processor is in the halt state.



NON MASKABLE INTERRUPT REQUEST OPERATION
FIGURE 4.0-6



HALT INSTRUCTION
IS RECEIVED
DURING THIS
MEMORY CYCLE

HALT EXIT
FIGURE 4.0-7

Absolute Maximum Ratings

Temperature Under Bias	Specified operating range
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{CC} .

$$I_{CC} = 200 \text{ mA}$$

Z80-CPU D.C. Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - 0.6$		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 1.8 \text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -250 \mu\text{A}$
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	$V_{OUT} = 2.4$ to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	$V_{OUT} = 0.4\text{V}$
I_{LD}	Data Bus Leakage Current in Input Mode			± 10	μA	$0 < V_{IN} < V_{CC}$

Capacitance

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_{cb}	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU

Ordering Information

C - Ceramic
P - Plastic
S - Standard 5V $\pm 5\%$ 0° to 70°C
E - Extended 5V $\pm 5\%$ -40° to 85°C
M - Military 5V $\pm 10\%$ -55° to 125°C

Z80A-CPU D.C. Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - 0.6$		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 1.8 \text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -250 \mu\text{A}$
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	$V_{OUT} = 2.4$ to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	$V_{OUT} = 0.4\text{V}$
I_{LD}	Data Bus Leakage Current in Input Mode			± 10	μA	$0 < V_{IN} < V_{CC}$

Capacitance

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_{cb}	Clock Capacitance	35	pt
C_{IN}	Input Capacitance	5	pt
C_{OUT}	Output Capacitance	10	pt

Z80A-CPU

Ordering Information

C - Ceramic
P - Plastic
S - Standard 5V $\pm 5\%$ 0° to 70°C

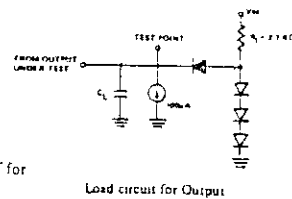
T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
φ	t _{CLK} (PH)	Clock Period	4	1121	nsec	
	t _{CLK} (PL)	Clock Pulse Width, Clock High	190	111	nsec	
	t _{CLK} (FL)	Clock Pulse Width, Clock Low	140	100	nsec	
	t _{CLK} (R)	Clock Rise and Fall Time		30	nsec	
A ₀₋₁₅	t _{DO} (AD)	Address Output Delay		145	nsec	C _L = 50pF
	t _{DF} (AD)	Delay to Float		110	nsec	
	t _{AS} (M)	Address Stable Prior to MREQ (Memory Cycle)	111		nsec	
	t _{AS} (R)	Address Stable Prior to IORQ, RD or WR (IO Cycle)	121		nsec	
	t _{AS} (F)	Address Stable From RD, WR, IORQ or MREQ	111		nsec	
D ₀₋₇	t _{DO} (D)	Data Output Delay		230	nsec	C _L = 50pF
	t _{DF} (D)	Delay to Float During Write Cycle		10	nsec	
	t _{DS} (D)	Data Setup Time to Rising Edge of Clock During M1 Cycle	70		nsec	
	t _{DS} (D)	Data Setup Time to Falling Edge of Clock During M2 to M5	70		nsec	
	t _{DS} (M)	Data Setup Prior to WR (Memory Cycle)	131		nsec	
	t _{DS} (R)	Data Setup Prior to RD (IO Cycle)	161		nsec	
	t _{DS} (W)	Data Setup Prior to WR	171		nsec	
H	t _H	Any Hold Time for Setup Time	0		nsec	
MREQ	t _{DM} (MR)	MREQ Delay From Falling Edge of Clock, MREQ Low		100	nsec	C _L = 50pF
	t _{DM} (MR)	MREQ Delay From Rising Edge of Clock, MREQ High		100	nsec	
	t _{DM} (MR)	MREQ Delay From Falling Edge of Clock, MREQ High		100	nsec	
	t _{WM} (MR)	Pulse Width, MREQ Low	181		nsec	
	t _{WM} (MR)	Pulse Width, MREQ High	191		nsec	
IORQ	t _{DI} (IR)	IORQ Delay From Rising Edge of Clock, IORQ Low		90	nsec	C _L = 50pF
	t _{DI} (IR)	IORQ Delay From Rising Edge of Clock, IORQ Low		110	nsec	
	t _{DI} (IR)	IORQ Delay From Rising Edge of Clock, IORQ High		100	nsec	
	t _{DI} (IR)	IORQ Delay From Falling Edge of Clock, IORQ High		110	nsec	
RD	t _{DR} (RD)	RD Delay From Rising Edge of Clock, RD Low		100	nsec	C _L = 50pF
	t _{DR} (RD)	RD Delay From Falling Edge of Clock, RD Low		130	nsec	
	t _{DR} (RD)	RD Delay From Rising Edge of Clock, RD High		100	nsec	
	t _{DR} (RD)	RD Delay From Falling Edge of Clock, RD High		110	nsec	
WR	t _{DR} (WR)	WR Delay From Rising Edge of Clock, WR Low		80	nsec	C _L = 50pF
	t _{DR} (WR)	WR Delay From Falling Edge of Clock, WR Low		90	nsec	
	t _{DR} (WR)	WR Delay From Falling Edge of Clock, WR High		100	nsec	
	t _{WR} (WR)	Pulse Width, WR Low	1101		nsec	
M1	t _{DM} (M1)	M1 Delay From Rising Edge of Clock, M1 Low		130	nsec	C _L = 50pF
	t _{DM} (M1)	M1 Delay From Rising Edge of Clock, M1 High		130	nsec	
RFSH	t _{DR} (RF)	RFSH Delay From Rising Edge of Clock, RFSH Low		180	nsec	C _L = 50pF
	t _{DR} (RF)	RFSH Delay From Rising Edge of Clock, RFSH High		150	nsec	
WAIT	t _W (WT)	WAIT Setup Time to Falling Edge of Clock	70		nsec	
HALT	t _D (HT)	HALT Delay Time From Falling Edge of Clock		300	nsec	C _L = 50pF
INT	t _S (IT)	INT Setup Time to Rising Edge of Clock	80		nsec	
NMI	t _W (NML)	Pulse Width, NMI Low	80		nsec	
BUSRD	t _S (BR)	BUSRD Setup Time to Rising Edge of Clock	80		nsec	
BUSAK	t _{DR} (BA)	BUSAK Delay From Rising Edge of Clock, BUSAK Low		120	nsec	C _L = 50pF
	t _{DR} (BA)	BUSAK Delay From Falling Edge of Clock, BUSAK High		110	nsec	
RESET	t _S (RS)	RESET Setup Time to Rising Edge of Clock	90		nsec	
	t _F (FC)	Delay to Float (MREQ, IORQ, RD and WR)		100	nsec	
t _{MR}	t _{MR}	M1 Stable Prior to IORQ (Interrupt Ack.)	1111		nsec	

- [12] t_{CL} = t_{W(ΦH)} + t_{W(ΦL)} + t_r + t_f
- [11] t_{dcM} = t_{W(ΦH)} + t_r - 75
- [12] t_{dcL} = t_r - 80
- [13] t_{dcH} = t_{W(ΦL)} + t_r - 40
- [14] t_{dcL} = t_{W(ΦL)} + t_r - 60
- [15] t_{dcM} = t_c - 210
- [16] t_{dcL} = t_{W(ΦL)} + t_r - 210
- [17] t_{dcH} = t_{W(ΦL)} + t_r - 30
- [18] t_{W(NML)} = t_c - 40
- [19] t_{W(NRH)} = t_{W(ΦH)} + t_r - 30
- [10] t_{W(WRL)} = t_c - 40
- [11] t_{MR} = 2t_c + t_{W(ΦH)} + t_r - 80

NOTES

- A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when M1 and IORQ are both active.
- B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.
- C. The RESET signal must be active for a minimum of 3 clock cycles.
- D. Output Delay vs. Loaded Capacitance
T_A = 20°C, V_{CC} = +5V ± 5%
Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines
- E. Although static by design, testing guarantees t_{W(ΦH)} of 200 nsec maximum



Load circuit for Output

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	$V_{CC} - 0.6V$	4.5V
OUTPUT	2.0V	8V
INPUT	2.0V	8V
FLOAT	ΔV	$\pm 0.5V$

$t_w(OL) \cdot t_r \cdot t_f$

$t_r - 75$

40

$t_r - 60$

$t_r - 210$

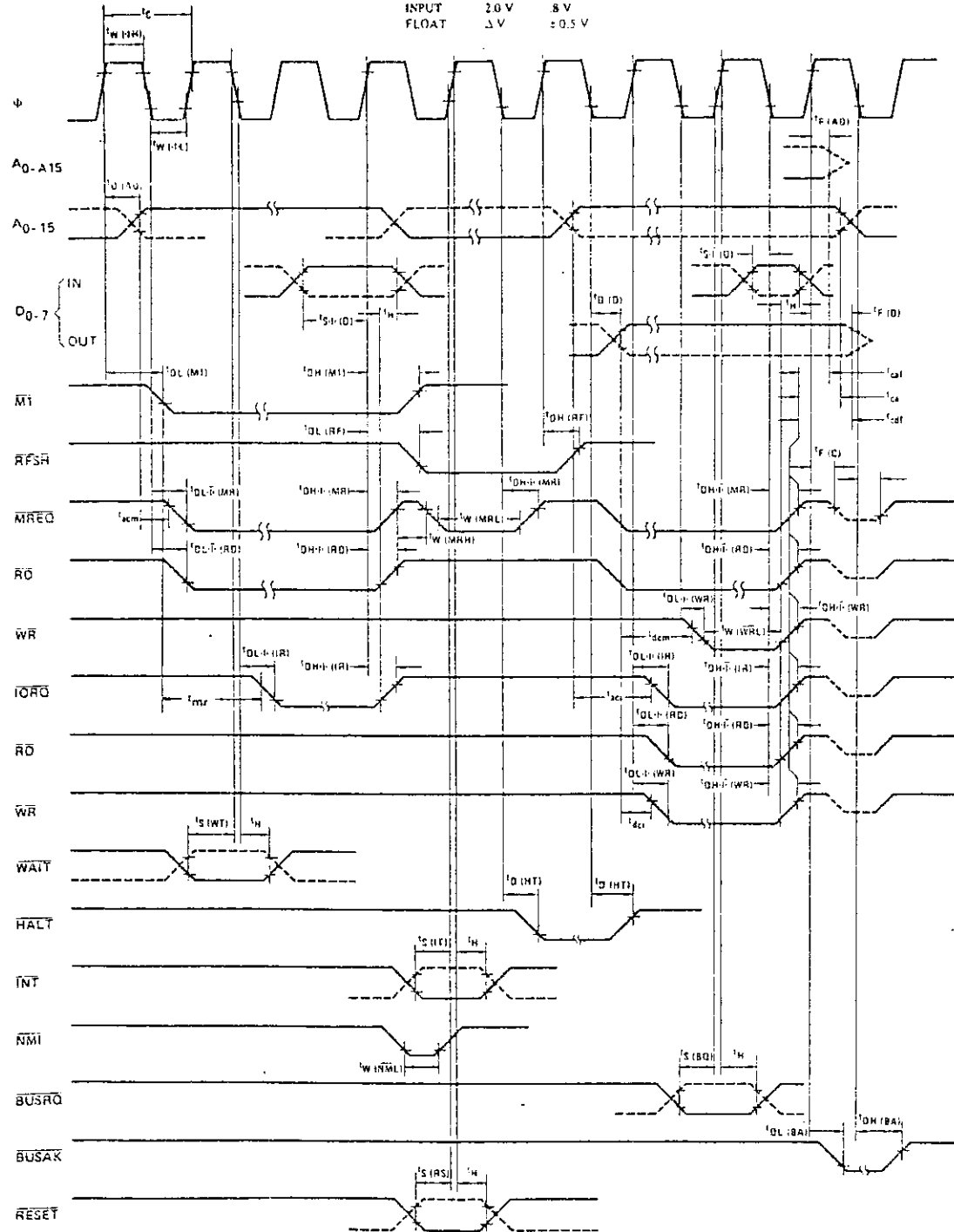
$t_r - 80$

40

$t_r - 30$

40

$t_r - 80$



T_A = 0°C to 70°C, V_{cc} = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
•	t _c	Clock Period	25	[12]	μsec	
	t _{w(ΦH)}	Clock Pulse Width, Clock High	110	[17]	nsec	
	t _{w(ΦL)}	Clock Pulse Width, Clock Low	110	2000	nsec	
	t _{r, f}	Clock Rise and Fall Time		30	nsec	
A ₀₋₁₅	t _{D(AD)}	Address Output Delay		110	nsec	C _L = 50pF
	t _{F(AD)}	Delay to Float		90	nsec	
	t _{acm}	Address Stable Prior to MREQ (Memory Cycle)	[18]		nsec	
	t _{aci}	Address Stable Prior to IORQ, RD or WR (I/O Cycle)	[21]		nsec	
	t _{caf}	Address Stable From RD, WR, IORQ or MREQ	[13]		nsec	
D ₀₋₇	t _{D(D)}	Data Output Delay		150	nsec	C _L = 50pF
	t _{F(D)}	Delay to Float During Write Cycle		90	nsec	
	t _{SD(D)}	Data Setup Time to Rising Edge of Clock During M1 Cycle	33		nsec	
	t _{SΦ(D)}	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t _{dcm}	Data Stable Prior to WR (Memory Cycle)	[15]		nsec	
	t _{dci}	Data Stable Prior to WR (I/O Cycle)	[16]		nsec	
	t _{dof}	Data Stable From WR	[17]		nsec	
	t _H	Any Hold Time for Setup Time		0	nsec	
MREQ	t _{DLΦ(MR)}	MREQ Delay From Falling Edge of Clock, MREQ Low		85	nsec	C _L = 50pF
	t _{DHΦ(MR)}	MREQ Delay From Rising Edge of Clock, MREQ High		85	nsec	
	t _{DLΦ(MR)}	MREQ Delay From Falling Edge of Clock, MREQ High		85	nsec	
	t _{w(MRL)}	Pulse Width, MREQ Low	[18]		nsec	
	t _{w(MRH)}	Pulse Width, MREQ High	[19]		nsec	
IORQ	t _{DLΦ(IR)}	IORQ Delay From Rising Edge of Clock, IORQ Low		75	nsec	C _L = 50pF
	t _{DHΦ(IR)}	IORQ Delay From Falling Edge of Clock, IORQ Low		85	nsec	
	t _{DLΦ(IR)}	IORQ Delay From Rising Edge of Clock, IORQ High		85	nsec	
	t _{DHΦ(IR)}	IORQ Delay From Falling Edge of Clock, IORQ High		85	nsec	
	t _{w(MRH)}	Pulse Width, MREQ High		85	nsec	
RD	t _{DLΦ(RD)}	RD Delay From Rising Edge of Clock, RD Low		85	nsec	C _L = 50pF
	t _{DHΦ(RD)}	RD Delay From Falling Edge of Clock, RD Low		93	nsec	
	t _{DLΦ(RD)}	RD Delay From Rising Edge of Clock, RD High		85	nsec	
	t _{DHΦ(RD)}	RD Delay From Falling Edge of Clock, RD High		85	nsec	
	t _{w(MRH)}	Pulse Width, MREQ High		85	nsec	
WR	t _{DLΦ(WR)}	WR Delay From Rising Edge of Clock, WR Low		65	nsec	C _L = 50pF
	t _{DHΦ(WR)}	WR Delay From Falling Edge of Clock, WR Low		30	nsec	
	t _{DLΦ(WR)}	WR Delay From Rising Edge of Clock, WR High		30	nsec	
	t _{w(WRL)}	Pulse Width, WR Low	[10]		nsec	
M1	t _{DL(M1)}	M1 Delay From Rising Edge of Clock, M1 Low		100	nsec	C _L = 50pF
	t _{DH(M1)}	M1 Delay From Rising Edge of Clock, M1 High		100	nsec	
RFSH	t _{DL(RF)}	RFSH Delay From Rising Edge of Clock, RFSH Low		130	nsec	C _L = 50pF
	t _{DH(RF)}	RFSH Delay From Rising Edge of Clock, RFSH High		120	nsec	
WAIT	t _{s(WT)}	WAIT Setup Time to Falling Edge of Clock	70		nsec	
HALT	t _{D(HT)}	HALT Delay Time From Falling Edge of Clock		300	nsec	
INT	t _{s(IT)}	INT Setup Time to Rising Edge of Clock	80		nsec	
NMI	t _{w(NML)}	Pulse Width, NMI Low	80		nsec	
BUSRQ	t _{s(BQ)}	BUSRQ Setup Time to Rising Edge of Clock	50		nsec	
BUSAK	t _{DL(BA)}	BUSAK Delay From Rising Edge of Clock, BUSAK Low		100	nsec	C _L = 50pF
	t _{DH(BA)}	BUSAK Delay From Falling Edge of Clock, BUSAK High		100	nsec	
RESET	t _{s(RS)}	RESET Setup Time to Rising Edge of Clock	60		nsec	
	t _{F(C)}	Delay to Float (MREQ, IORQ, RD and WR)		80	nsec	
	t _{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

[12] t_c = t_{w(ΦH)} + t_{w(ΦL)} + t_r + t_f

[11] t_{acm} = t_{w(ΦH)} + t_r - 65

[2] t_{aci} = t_c - 70

[3] t_{ca} = t_{w(ΦL)} + t_r - 50

[4] t_{caf} = t_{w(ΦL)} + t_r - 45

[5] t_{dcm} = t_c - 170

[6] t_{dci} = t_{w(ΦL)} + t_r - 170

[7] t_{cdf} = t_{w(ΦL)} + t_r - 70

[8] t_{w(MRL)} = t_c - 30

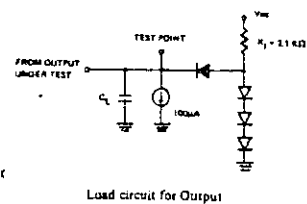
[9] t_{w(MRH)} = t_{w(ΦH)} + t_r - 20

[10] t_{w(WRL)} = t_c - 30

[11] t_{mr} = 2t_c + t_{w(ΦH)} + t_r - 65

NOTES:

- A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when M1 and IORQ are both active.
- B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.
- C. The RESET signal must be active for a minimum of 3 clock cycles.
- D. Output Delay vs. Loaded Capacitance
T_A = 70°C V_{cc} = +5V ± 5%
Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.
- E. Although static by design, testing guarantees t_{w(ΦH)} of 200 μsec maximum



Load circuit for Output

Especificações Técnicas da ROM IC3

250K

207561
10/20/80

262,144 BIT STATIC READ ONLY MEMORY

FEATURES:

- 32,768 x 8 organization
- Single +5V \pm 10% supply
- 450ns max access time: RD9256B
- 350ns max access time: RD9256CS
- 300ns max access time: RD9256C
- 250ns max access time: RD9256DS
- 200ns max access time: RD9256D
- Totally static operation
- Three state outputs
- All TTL compatible input/outputs
- 28 Pin JEDEC approved package: RD9256
- Programmable "FlexSelect"™ chip enable/disable/power down capabilities controlled by the chip enable (CE) and output enable (OE) inputs
- ESD Protection: Inputs are designed to meet 2.3KV per Test method 3015.1, MIL-STD883B

DESCRIPTION

The General Instrument RD9256 is a 262,144 Bit Static Read Only Memory organized as 32,768 eight-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RD9256 provides the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation.

Operation

Address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive logic address is decoded on-chip to select on the 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most significant bit of the word address.

Chip Select

Chip enable/disable/power down "FlexSelect"™. These inputs can be programmed during mask fabrication to implement various logic functions which provides the designer with a flexible and easy means of "chip selecting" and/or "powering down" the device. The "FlexSelect"™ options are on the following pages.

PIN CONFIGURATION

28 LEAD DUAL-IN-LINE

RD9256

Top View

N.C.	1	28	V _{CC}
A12	2	27	A14
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE/CS1
A2	8	21	A10
A1	9	20	CE/CS2
A0	10	19	O8
O1	11	18	O7
O2	12	17	O6
O3	13	16	O5
GND	14	15	O4

1) Standard Chip Select requirements - Non-Power Down

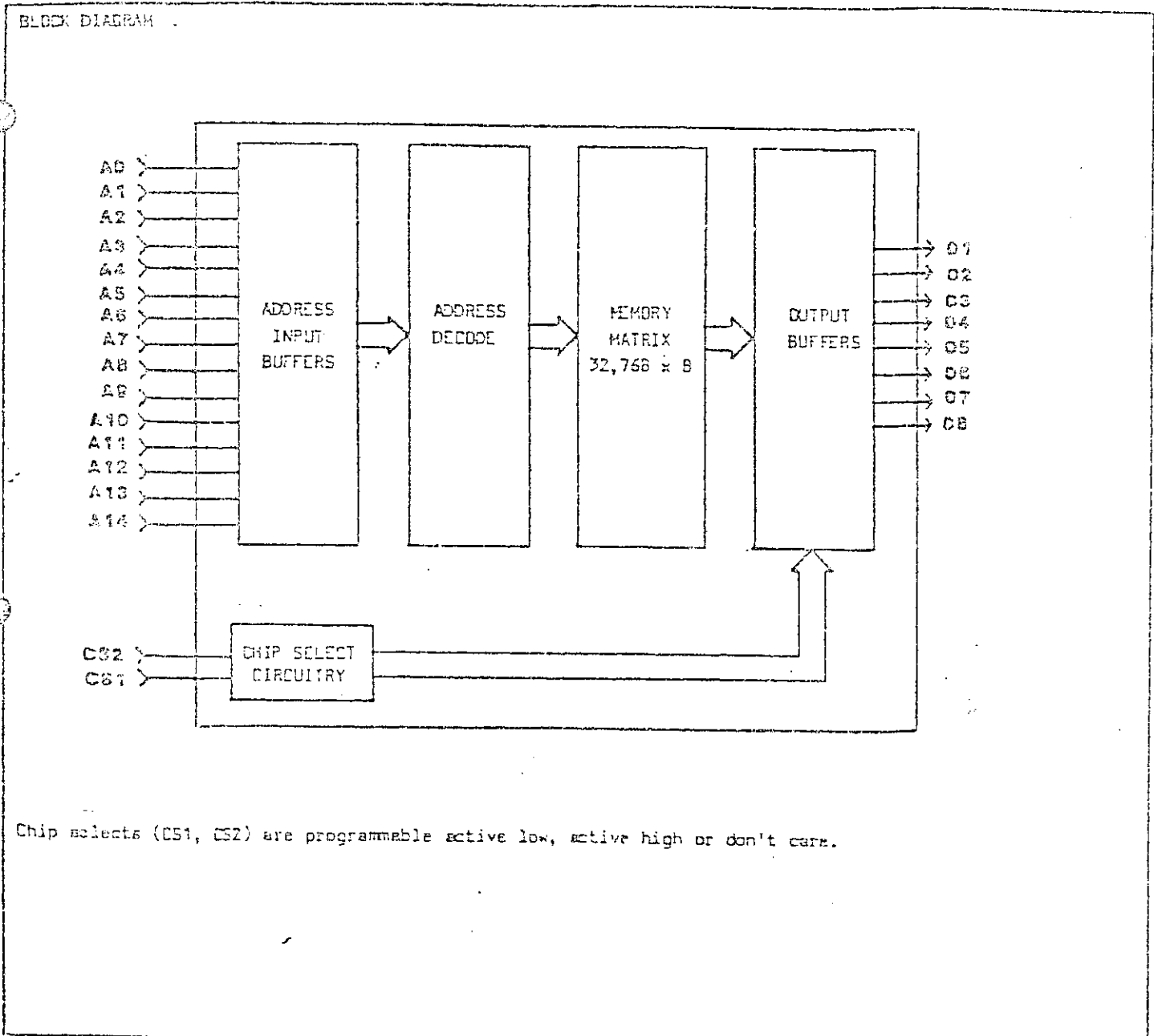
CS1 = 0,1 or don't care (Pin 22)

CS2 = 0,1 or don't care (Pin 20)

Logic Function $\overline{1}(CS1) \cdot \overline{1}(CS2) = \text{Chip Selected}$

$\overline{1}$ Programmed in active state

"." = Logical "AND"

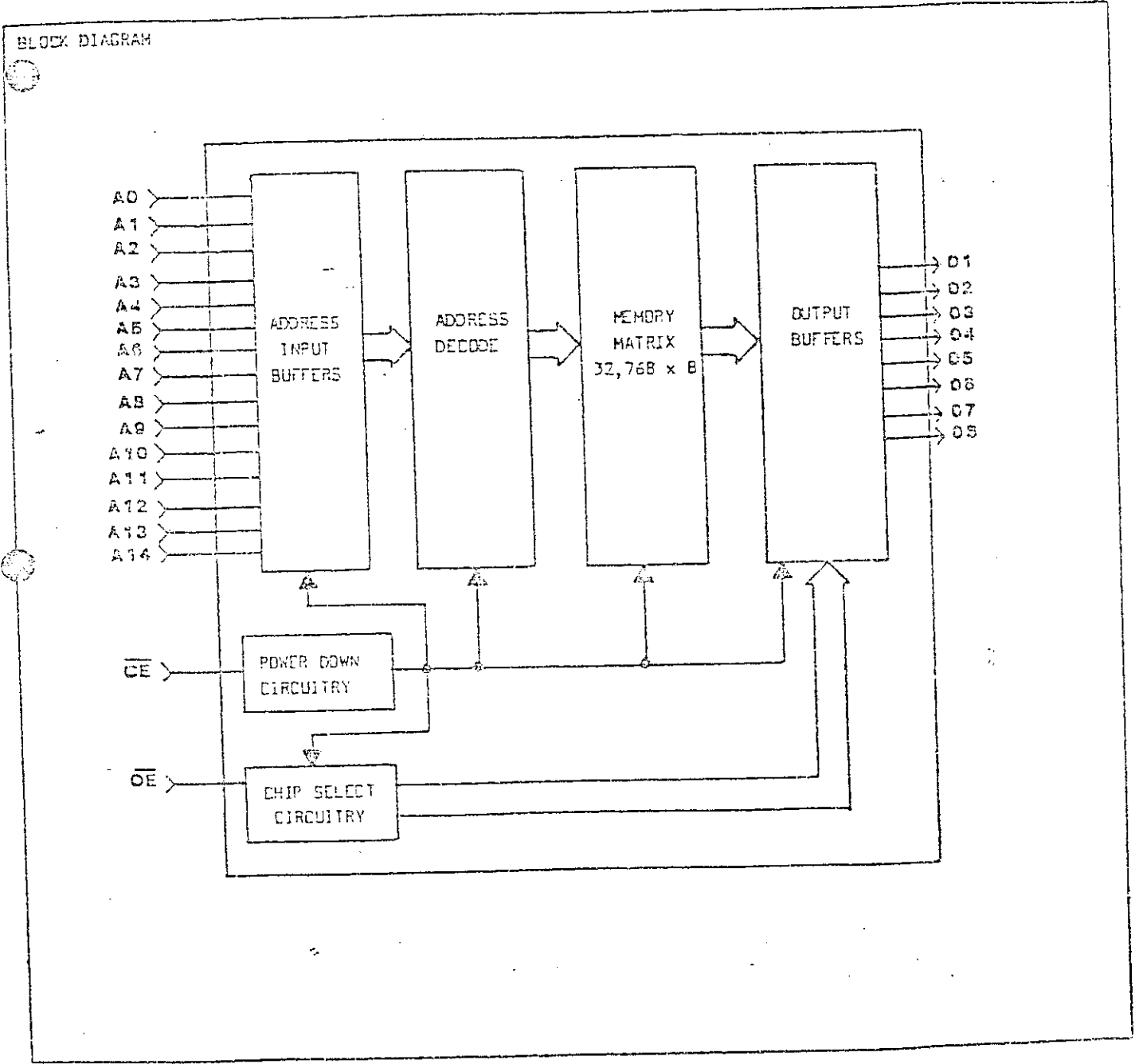


11) Standard Chip Select requirements - Power Down

\overline{OE} (Pin 22) When \overline{CE} goes high, the device will automatically power down and remain in a low power standby mode as long as \overline{CE} remains high. The \overline{OE} function eliminates bus contention in multiple memory device systems.

Logic Function: $(\overline{CE}) \cdot (\overline{OE}) = \text{Chip Selected}$

"." = LOGICAL "AND"

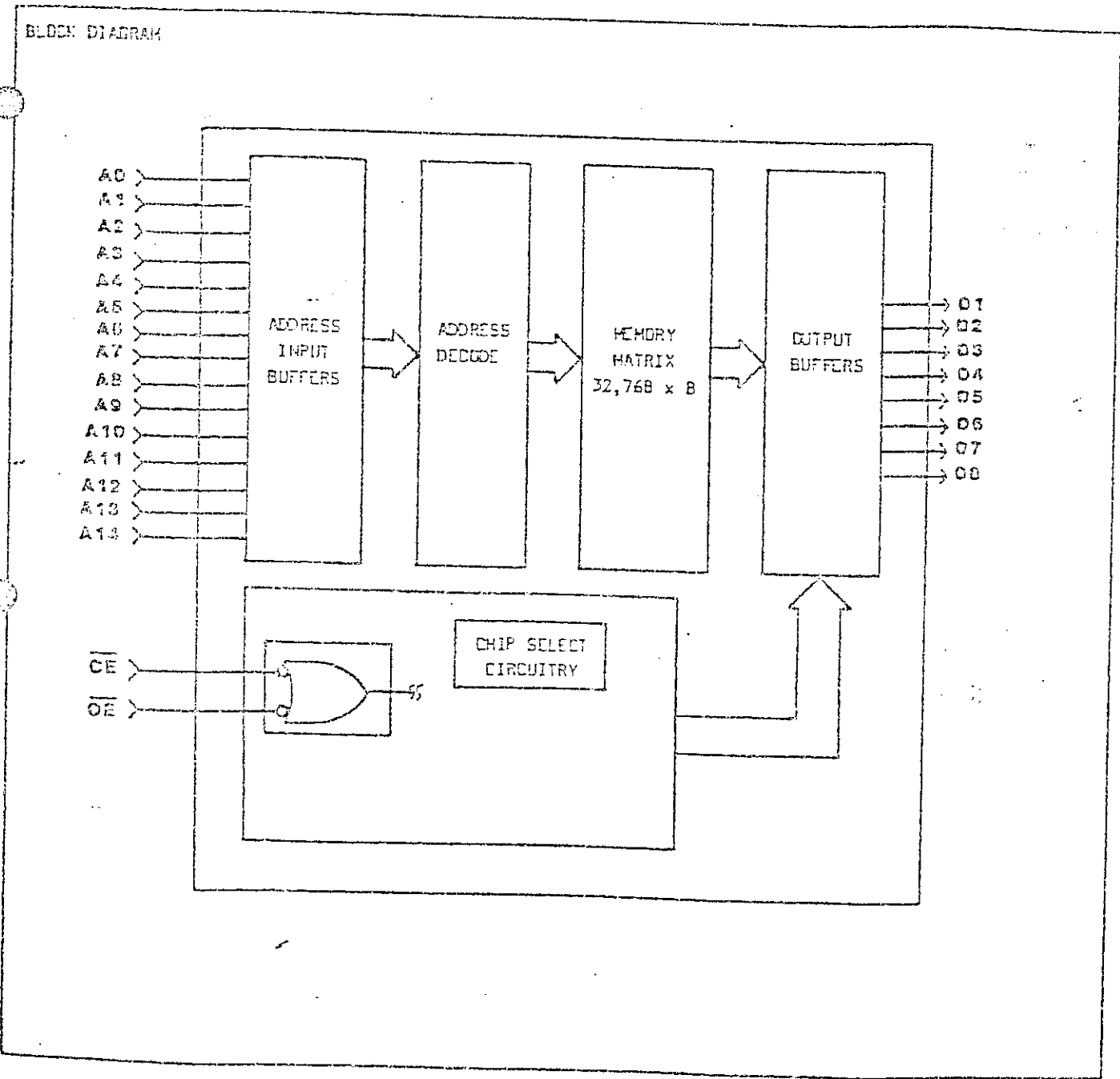


111) "DDED" chip select requirement (chip selects at pins 20 (\overline{CE}) and 22 (\overline{OE}) function as a logical "OR").

*This is ideally suited for applications that have limited chip select decoding capabilities.

Logic Function: $(\overline{CE} + \overline{OE}) = \text{Chip Selected}$

"+" = LOGICAL "OR"



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages
(with Respect to GND)..... -0.5V to +7.0V
Storage Temperature..... -65°C to +150°C

Standard Conditions (unless otherwise noted):

V_{CC} = 5V ±10%
Operating Temperature T_A = 0°C to +70°C
Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}/\overline{CS2}$, $\overline{CE}/\overline{CS1}$						
Inputs						
Logic "1"	V _{IH}	2.0	-	V _{CC}	V	V _{IH} = 0.4V to V _{CC}
Logic "0"	V _{IL}	-0.3	-	0.8	V	
Leakage	I _{LI}	-10	-	+10	µA	
Data Outputs						
Logic "1"	V _{OH}	2.4	-	V _{CC}	V	I _{OH} = -400µA
Logic "0"	V _{OL}	-	-	0.4	V	I _{OL} = 3.2mA
Leakage	I _{LO}	-10	-	+10	µA	V _{OUT} = 0.4V to V _{CC}
Power Supply Current						
I _{CC} (Active)	-	-	-	100	mA	Note 1
I _{CC} (Standby)	-	-	-	20	mA	Note 2

AC CHARACTERISTICS

Characteristics	Sym	R09256B		R09256CS		R09256C		R09256DS		R09256D		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address Access Time	t _{ACC}	-	450	-	350	-	300	-	250	-	200	ns	
Address Hold After Address Change	t _{CH}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Chip Enable Time	t _{ACE}	-	450	-	350	-	300	-	250	-	200	ns	
Chip Select, Output Enable Access Time	t _{ACS}	-	150	-	125	-	100	-	85	-	70	ns	Note 4
Output Disable Time	t _{OFF}	-	150	-	125	-	100	-	85	-	70	ns	
Output Low Z Delay	t _{LZ}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Output High Z Delay	t _{HZ}	-	150	-	125	-	100	-	85	-	70	ns	Note 5
Capacitance***													
Input Capacitance	C _I	-	7	-	7	-	7	-	7	-	7	pf	F = 1MHz, T _A = +25°C
Output Capacitance	C _O	-	10	-	10	-	10	-	10	-	10	pf	F = 1MHz, T _A = +25°C

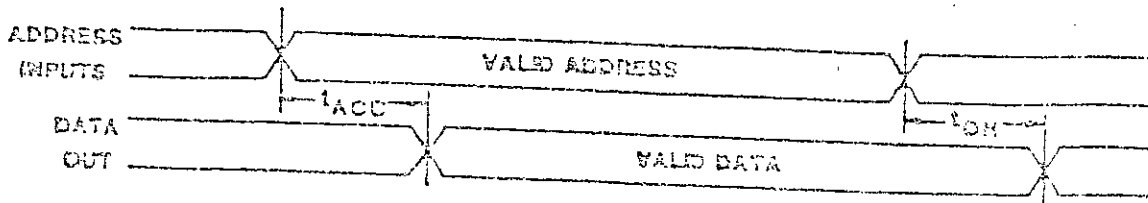
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

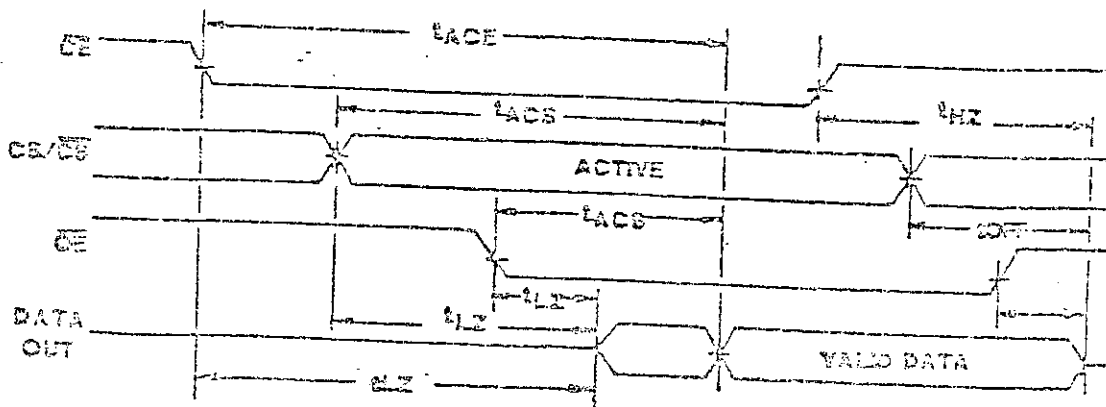
1. Measured with device selected and outputs unloaded.
2. Device disabled with $\overline{CE} \geq 2.0V$ ("Power Down" programmed parts only).
3. These parameters are periodically sampled and not 100% tested.
4. Access time to valid data measured from $\overline{CS1}$ going active and/or \overline{OE} going low whichever occurs last/first.
5. Output high impedance delay (t_{HZ}) is measured from \overline{CE} and/or \overline{OE} going high or $\overline{CS1}$ going active, whichever occurs first/last.

TIMING DIAGRAMS

Propagation Delay from Address: $\overline{CE} = \overline{OE} = LDR, LS/\overline{CS} = \text{Active}$



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels.....	0.4V to 2.4V
Input Rise and Fall Times.....	5/10ns
Timing Measurement Levels: Input/Output..	0.8V AND 2.0V
Output Load.....	See Figure 1

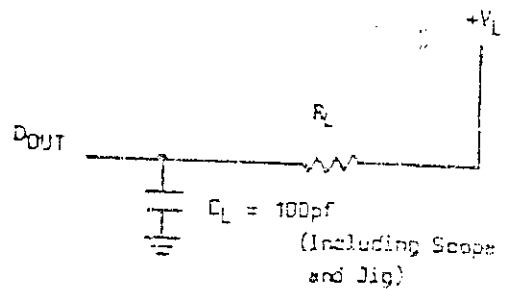


Fig. 1

NORTH AMERICA

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NORTH EAST - 600 West 100th Street
Pickering, Ont. L1V 1B7
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730 Highway 14, Suite 104
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Tel: (201) 294-1524 TWX: 710-480-1449

SOUTHEAST - 1516 Forest Drive
Anniston, Michigan 49403
Tel: (501) 256-4240 TWX: 710-257-4258
19 West Market Street, Suite 209E
Raleigh, North Carolina 27601
Tel: (919) 823-0211
3157 Coble Open Court
Durham, NC 27706
Tel: (404) 474-0274

SOUTH CENTRAL - 4225 LBJ Frey, Suite 205
Dallas, Texas 75234
Tel: (214) 324-1524 TWX: 910-420-1528

CENTRAL - 2524 S. Michigan Street
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6011 East 52nd Street, Suite A
Indianapolis, Indiana 46220
Tel: (317) 261-5571 TWX: 810-241-2145
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Arlington Heights, Illinois 60005
Tel: (312) 981-0340
730 North River Road, Suite 118
Burlington, Minnesota 55307
Tel: (612) 264-1540 TWX: 950-575-0240

SOUTHWEST - 201 Standard Street
El Segundo, California 90245
Tel: (213) 227-7745 TWX: 910-268-0245

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San Diego, California 92101
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111-5 Singapore Street
Singapore 060001-1011 Telex: 813
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KOREA:

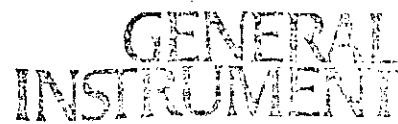
GENERAL INSTRUMENT MICROELECTRONICS
AND TANG BUILDING 1204
51-4 Seokcho-Dong
Chongno-Pu, Seoul, Korea
Tel: (2) 744-4543 Telex: K. 2740 DAEMO

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Level 1214, Shaw Centre
1 Scotts Road, Singapore 2222
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TAIWAN:

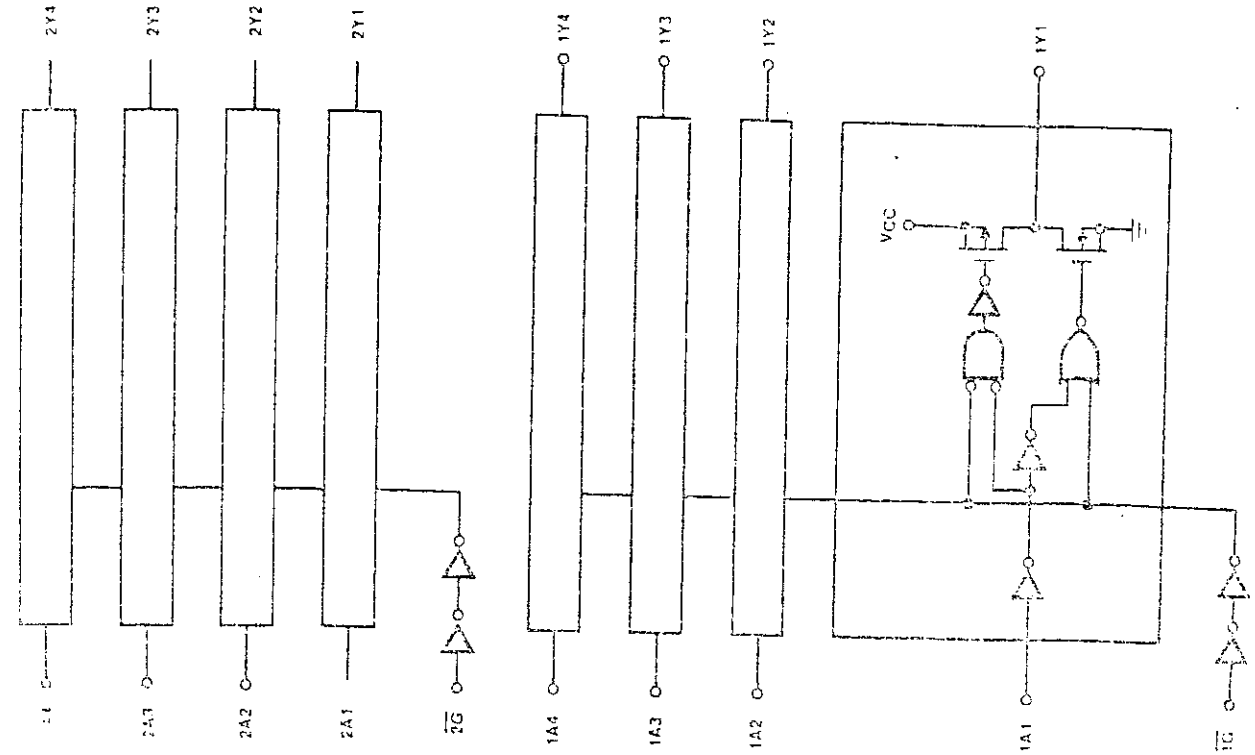
GENERAL INSTRUMENT
MICROELECTRONICS TAIWAN
233 Pao Chiao Road, Hsin-Tsin
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Especificações Técnicas do IC 5 - 74LS244 -

HC244



AC Electrical Characteristics (V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits
t _{PLH} -t _{PLZ}	Maximum Propagation Delay	C _L = 45 pF	14	20
t _{ZH} -t _{ZL}	Maximum Enable Delay to Active Output	R _L = 1 kΩ C _L = 45 pF	17	28
t _{FZH} -t _{FZL}	Maximum Enable Delay from Active Output	R _L = 1 kΩ C _L = 5 pF	15	25

AC Electrical Characteristics (V_{CC} = 2.0V-3.0V, C_L = 50 pF, t_{PLH} = t_{PLZ} = 6 ns (unless otherwise specified))

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		Guaranteed Limits	
				Typ	Max	74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C
t _{PLH} -t _{PLZ}	Maximum Propagation Delay	C _L = 50 pF	2.0V	59	115	145	171
		C _L = 150 pF	2.0V	83	165	203	246
		C _L = 50 pF	4.5V	14	23	29	34
		C _L = 150 pF	4.5V	17	33	42	49
		C _L = 50 pF	6.0V	10	20	25	29
		C _L = 150 pF	6.0V	14	28	35	42
t _{FZH} -t _{FZL}	Maximum Output Enable Time	R _L = 1 kΩ					
		C _L = 50 pF	2.0V	75	780	169	224
		C _L = 150 pF	2.0V	100	200	252	293
		C _L = 50 pF	4.5V	15	30	38	45
		C _L = 150 pF	4.5V	20	40	50	60
		C _L = 50 pF	6.0V	13	28	32	38
t _{FZH} -t _{FZL}	Maximum Output Disable Time	C _L = 150 pF	2.0V	17	21	43	51
		C _L = 50 pF	2.0V	75	150	189	224
		C _L = 150 pF	2.0V	15	20	35	45
t _{PLH} -t _{PHL}	Maximum Output Rise and Fall Time	C _L = 50 pF	2.0V	13	25	32	38
		C _L = 150 pF	2.0V	60	75	75	80
		C _L = 50 pF	4.5V	12	12	15	16
C _{PD}	Power Dissipation Capacitance (Notes 5)	C _L = 50 pF	2.0V	10	10	10	10
		C _L = 150 pF	2.0V	5	5	5	5
		C _L = 50 pF	6.0V	10	10	10	10
C _{IN}	Maximum Input Capacitance			10	10	10	10
				10	10	10	10
C _{OUT}	Maximum Output Capacitance			10	10	10	10
				10	10	10	10

Note 5: C_{PD} determines the no load dynamic power consumption. P_Q = C_{PD} V_{CC} f + I_{CC} V_{CC} and the no load dynamic current consumption.

Motorola MCM54HC244/MCM74HC244 CMOS TRI-STATE® Buffer

microCMOS

General Description

These TRI-STATE buffers utilize microCMOS technology. 3.5 micron silicon gate P-well CMOS, and are general purpose high speed non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantages of CMOS circuitry: i.e., high noise immunity, and low power consumption. All devices have a fan-out of 15 LS-TTL equivalent inputs.

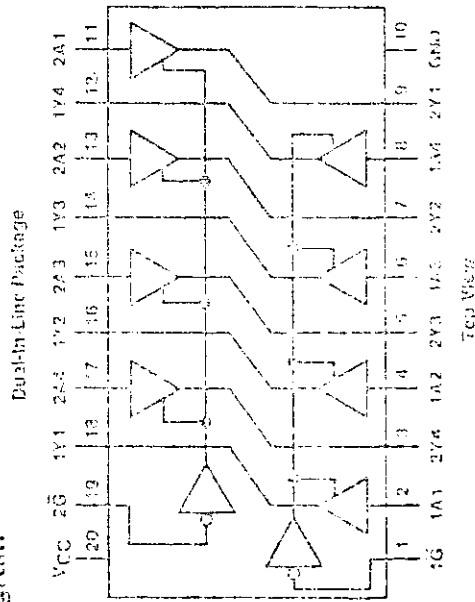
The MCM54HC244/MCM74HC244 is a non-inverting buffer and it is two active low enables (1G and 2G). Each enable is independently controlled by buffers. This device does not have Schottky trigger inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2-5V
- Low quiescent supply current: 60 µA (74 Series)
- Output current: 6 mA

Connection Diagram



Order Number MCM54HC244 or MCM74HC244
See NS Package Catalog for MCM

Truth Table

1G	1A	1Y	1Z	2A	2Y
L	L	L	L	L	L
L	H	L	L	H	H
H	L	L	L	L	L
H	L	Z	L	L	Z

HC244

Maximum Ratings (Note 1 & 2)

Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V _I , V _O)	-1.5 to V _{CC} + 1.5V
Operating Temperature Range (T _{stg})	-65°C to +150°C
Storage Temperature Range (T _{stg})	-65°C to +150°C
Power Dissipation (P _D)	500 mW (typical)
Operating Temperature Range (T _{op})	-55°C to +125°C

Operating Conditions

Supply Voltage (V _{CC})	Min: 2, Max: 6
DC Input or Output Voltage (V _I , V _O)	Min: 0, Max: V _{CC}
Operating Temperature Range (T _{op})	Min: -55, Max: +125
Input Rise or Fall Times (t _r , t _f)	Min: 1000 ns, Max: 500 ns
Output Current (I _O)	Min: 0, Max: 400

Electrical Characteristics (Note 4)

Parameter	Conditions	V _{CC}	T _A = 25°C		74HC T _A = -40 to 85°C		54HC T _A = -55 to 125°C		Units
			Typ	Max	Min	Max	Min	Max	
Minimum High Level Input Voltage	V _{IH} = V _{IH} or V _I I _O = 0 µA	2.0V	1.5	1.5	1.5	1.5	1.5	V	
Maximum Low Level Input Voltage	V _{IL} = V _{IL} or V _I I _O = 0 µA	4.5V	3.15	3.15	3.15	3.15	3.15	V	
Minimum High Level Output Voltage	V _{IH} = V _{IH} or V _I I _O = 20 µA	5.0V	4.2	4.2	4.2	4.2	4.2	V	
Maximum Low Level Output Voltage	V _{IL} = V _{IL} or V _I I _O = 20 µA	2.0V	0.9	0.9	0.9	0.9	0.9	V	
Minimum High Level Output Voltage	V _{IH} = V _{IH} or V _I I _O = 20 µA	4.5V	0.8	0.8	0.8	0.8	0.8	V	
Maximum Low Level Output Voltage	V _{IL} = V _{IL} or V _I I _O = 20 µA	6.0V	1.2	1.2	1.2	1.2	1.2	V	
Minimum Input Current	V _{IH} = V _{IH} or V _I I _O = 0 µA	2.0V	0	0	0	0	0	µA	
Maximum Input Current	V _{IL} = V _{IL} or V _I I _O = 0 µA	4.5V	4.2	3.98	3.84	3.7	3.7	µA	
Maximum Output Current	V _{IH} = V _{IH} or V _I I _O = 0 µA	6.0V	5.7	5.48	5.34	5.2	5.2	µA	
Maximum Output Current	V _{IH} = V _{IH} or V _I I _O = 0 µA	2.0V	0	0	0	0	0	µA	
Maximum Output Current	V _{IL} = V _{IL} or V _I I _O = 0 µA	4.5V	0.2	0.26	0.33	0.4	0.4	µA	
Maximum Output Current	V _{IL} = V _{IL} or V _I I _O = 0 µA	6.0V	0.2	0.26	0.33	0.4	0.4	µA	
Maximum Output Current	V _{IH} = V _{IH} or V _I I _O = 0 µA	6.0V	±0.1	±0.1	±0.1	±0.1	±0.1	µA	
Maximum Output Current	V _{IL} = V _{IL} or V _I I _O = 0 µA	6.0V	±0.5	±0.5	±0.5	±0.5	±0.5	µA	
Maximum Output Current	V _{IH} = V _{IH} or V _I I _O = 0 µA	6.0V	8.0	8.0	8.0	8.0	8.0	µA	

Note 1: All voltages are with respect to ground.

Note 2: All currents are with respect to ground.

Note 3: All currents are with respect to ground.

Note 4: All currents are with respect to ground.

Note 5: All currents are with respect to ground.

Note 6: All currents are with respect to ground.

Note 7: All currents are with respect to ground.

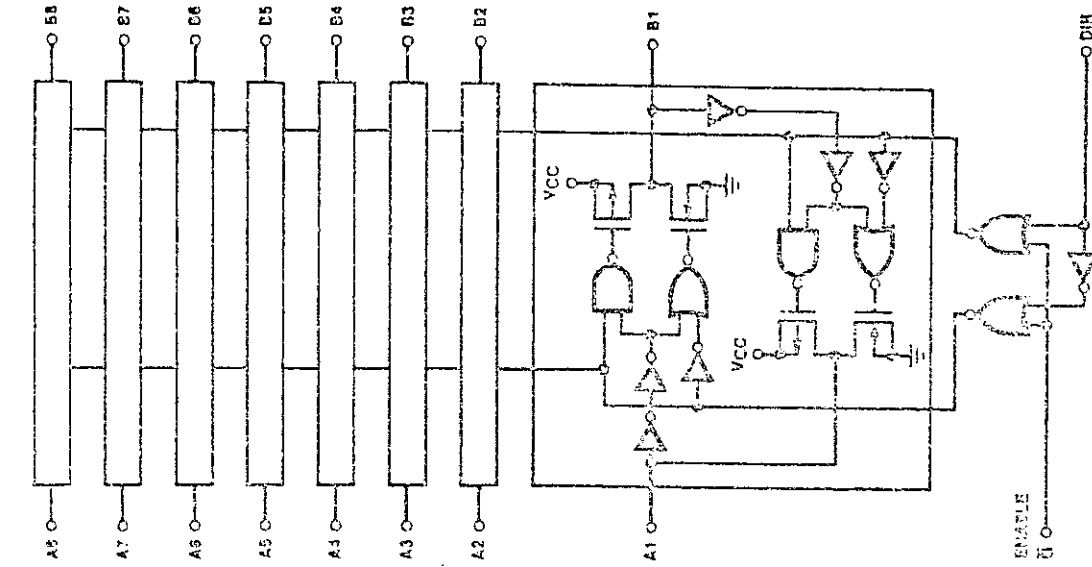
Note 8: All currents are with respect to ground.

Note 9: All currents are with respect to ground.

Note 10: All currents are with respect to ground.

Especificações Técnicas do IC 4 - 74LS245 -

Logic Diagram



TUJF16105-2

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, t_r = t_f = 6 ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 45 pF$	13	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 45 pF$	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 5 pF$	32	42	ns

AC Electrical Characteristics $V_{CC} = 2.0V \text{ to } 6.0V, C_L = 50 pF, t_r = t_f = 6 ns$ (unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC}	TA = 25°C		74HC TA = -40 to 85°C		54HC TA = -55 to 125°C	
				Typ	Guaranteed Limits	Typ	Guaranteed Limits	Typ	Guaranteed Limits
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50 pF$	2.0V	20	72	83	96		
		$C_L = 150 pF$	2.0V	38	96	113	128		
		$C_L = 50 pF$	4.5V	14	19	22	24		
		$C_L = 150 pF$	4.5V	18	24	29	32		
		$C_L = 50 pF$	6.0V	14	16	22	24		
		$C_L = 150 pF$	6.0V	18	24	29	32		
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$							
		$C_L = 50 pF$	2.0V	70	184	224	240		
		$C_L = 150 pF$	2.0V	80	216	260	284		
		$C_L = 50 pF$	4.5V	35	46	56	60		
		$C_L = 150 pF$	4.5V	41	54	65	71		
		$C_L = 50 pF$	6.0V	31	41	50	54		
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$C_L = 150 pF$	6.0V	36	47	57	62		
		$R_L = 1 k\Omega$	2.0V	47	172	206	224		
		$C_L = 50 pF$	4.5V	30	43	52	56		
t_{RHL}, t_{FHL}	Output Rise and Fall Time	$C_L = 50 pF$	2.0V	20	60	75	80		
			4.5V	6	12	15	18		
			6.0V	5	10	13	15		
C _{PD}	Power Dissipation	$\bar{G} = V_{IL}$		100					
		$\bar{G} = V_{IH}$		12					
C _{IN}	Minimum Input Capacitance			5	10	10	10		
C _{IN/OUT}	Maximum Input/Output Capacitance, A or B			15	20	20	20		

Note 5: C_{PD} determines the no load dynamic power consumption, P_Q = C_{PD}V_{CC}²/f. f is the frequency of the signal. C_{IN} and C_{IN/OUT} are the no load dynamic current consumption, I_S = C_{IN}dV/dt.

74HC245

MM54HC245/KM74HC245

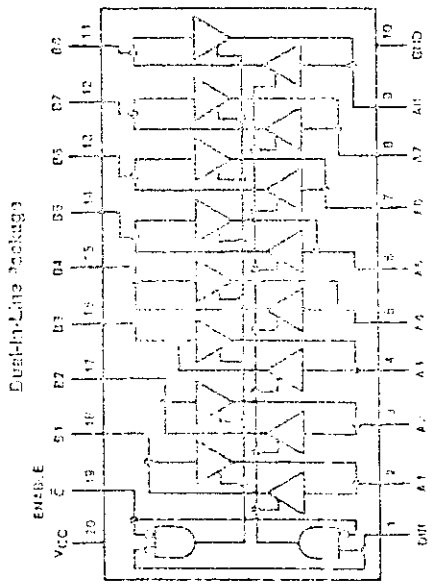
Octal TRI-STATE® Transceiver

General Description

This TRI-STATE bidirectional buffer is a CMOS Technology 3.5 micron silicon gate P-well CMOS, and is intended for bi-way asynchronous communication between data buses. It has high drive current capability which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device is an active low enable input \bar{G} and a direction control input \bar{D} . When \bar{D} is high, data flows from the A inputs to the B outputs. When \bar{D} is low, data flows from the B inputs to the A outputs. The MM54HC245/MM74HC245 transfers true data from one bus to the other.

Connection Diagram



Order Number MM54HC245J or MM74HC245J, N See MS Package 009A or 025A

Truth Table

Control Inputs		Operation
\bar{G}	\bar{D}	
L	L	0 data to A Bus
L	H	A data to B Bus
H	X	High-Z Bus Isolation

Static Maximum Ratings (Notes 1 & 2)

- V_{CC} -0.5 to +7.0V
- V_{OH} (5 pin) and \bar{G} pins (V_{OH}) -1.5 to V_{CC} +1.5V
- V_{OL} (I_{OL}) and \bar{G} pins (V_{OL}) -0.5 to V_{CC} +0.5V
- I_{CC} Current (I_{CC}) ±20 mA
- I_{OH} Current, per pin (I_{OH}) ±35 mA
- I_{OL} Current, per pin (I_{OL}) ±70 mA
- Temperature Range (T_{STG}) -65°C to +150°C
- Power Dissipation (P_D) (Notes 3) 500 mW
- Temp (T_J) (Soldering 10 seconds) 260°C

Operating Conditions

- Supply Voltage (V_{CC}) Min 2 Max 6
- DC Input or Output Voltage (V_{IH}, V_{OHT}) 0 V_{CC}
- Operating Temp. Range (T_A) MM74HC -40 +85 °C MM54HC -55 +125 °C
- Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V 1000 ns V_{CC}=4.5V 500 ns V_{CC}=6.0V 400 ns

Electrical Characteristics (Note 4)

Parameter	Conditions	V _{CC}	TA = 25°C		74HC	54HC	Units
			Typ	Max	TA = -40 to 85°C	TA = -55 to 125°C	
Minimum High Level Input Voltage	V _{IH} = V _{IH} or V _{IL} I _{OH} ≤ 20 μA	2.0V	1.5	1.5	1.5	1.5	V
		4.5V	3.15	3.15	3.15	3.15	V
		6.0V	4.2	4.2	4.2	4.2	V
Maximum Low Level Input Voltage	V _{IL} = V _{IH} or V _{IL} I _{OH} ≤ 20 μA	2.0V	0.3	0.3	0.3	0.3	V
		4.5V	0.9	0.9	0.9	0.9	V
		6.0V	1.2	1.2	1.2	1.2	V
Minimum High Level Output Voltage	V _{IH} = V _{IH} or V _{IL} I _{OH} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
		4.5V	4.5	4.4	4.4	4.4	V
		6.0V	6.0	5.9	5.9	5.9	V
Maximum Low Level Output Voltage	V _{IL} = V _{IH} or V _{IL} I _{OH} ≤ 20 μA	2.0V	0	0	0	0	V
		4.5V	0	0	0	0	V
		6.0V	0	0	0	0	V
Minimum High Level Output Voltage	V _{IH} = V _{IH} or V _{IL} I _{OH} ≤ 7.8 mA	2.0V	0	0	0	0	V
		4.5V	0.2	0.26	0.33	0.4	V
		6.0V	0.2	0.26	0.33	0.4	V
Maximum Low Level Output Voltage	V _{IL} = V _{IH} or V _{IL} I _{OH} ≤ 7.8 mA	2.0V	±0.1	±1.0	±1.0	±1.0	μA
		4.5V	±0.5	±5.0	±5.0	±5.0	μA
		6.0V	±0.5	±5.0	±5.0	±5.0	μA

1. Maximum junction temperature is 150°C.

2. Maximum power dissipation is 500 mW.

3. Power dissipation is based on a 10% duty cycle.

4. All values are typical at TA = 25°C.

5. All values are typical at TA = 25°C.

6. All values are typical at TA = 25°C.

Especificações Técnicas do IC 13,14 - 74LS157 -

Absolute Maximum Ratings (Notes 1 & 2)

- Supply Voltage (V_{CC}) -0.5 to +7.0V
- DC Input Voltage (V_{IN}) -1.5 to V_{CC} + 1.5V
- DC Output Voltage (V_{OUT}) -0.5 to V_{CC} + 0.5V
- Clamp Diode Current (I_{IK}, I_{OK}) ±20 mA
- DC Output Current, per pin (I_{OUT}) ±25 mA
- DC V_{CC} or GND Current, per pin (I_{CC}) ±60 mA
- Storage Temperature Range (T_{STG}) -65°C to +150°C
- Power Dissipation (P_D) (Notes 3)
- Lead Temp. (T_L) (Soldering 10 seconds) 280°C

Operating Conditions

- Supply Voltage (V_{CC}) Min 5V
- DC Input or Output Voltage (V_{IN}, V_{OUT}) 0
- Operating Temp. Range (T_A) Max 125°C
- MM74HC -40
- MM54HC -55
- Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V
- V_{CC} = 4.5V
- V_{CC} = 6.0V

DC Electrical Characteristics (Notes 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C
				Typ	Guaranteed Limits		
V _{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	1.5
			4.5V	3.15	3.15	3.15	3.15
			6.0V	4.2	4.2	4.2	4.2
V _{IL}	Maximum Low Level Input Voltage		2.0V	0.3	0.3	0.3	0.3
			4.5V	0.9	0.9	0.9	0.9
			6.0V	1.2	1.2	1.2	1.2
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9
			4.5V	4.5	4.4	4.4	4.4
			6.0V	6.0	5.9	5.9	5.9
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.84	3.7	3.7
			6.0V	5.7	5.34	5.2	5.2
			2.0V	0	0.1	0.1	0.1
I _{IN}	Maximum Input Current	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 50 μA	4.5V	0	0.1	0.1	0.1
			6.0V	0	0.1	0.1	0.1
			2.0V	0	0.1	0.1	0.1
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	4.5V	0.2	0.36	0.36	0.4
			6.0V	0.2	0.48	0.48	0.4
			2.0V	±0.1	±1.0	±1.0	±1.0

Note 1: Refer to Maximum Ratings and Power Values beyond which damage to the device may occur.
 Note 2: Unless otherwise specified, all voltages are referenced to ground.
 Note 3: Power dissipation is based on maximum junction temperature of 125°C for MM74HC and 100°C for MM54HC.
 Note 4: For a load capacitance of 50 pF, the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V, T_A = 25°C, t_r = t_f = 10 ns, and for HC at 6.0V, T_A = 25°C, t_r = t_f = 10 ns. For HC at 2.0V, T_A = 25°C, t_r = t_f = 10 ns, the worst case V_{OH} and V_{OL} occur at V_{CC} = 4.5V and 6.0V respectively. (The V_{OH} value at 5.5V and 6.0V is the worst case value for CMOS at the higher voltage and the 6.0V value is used.)

Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

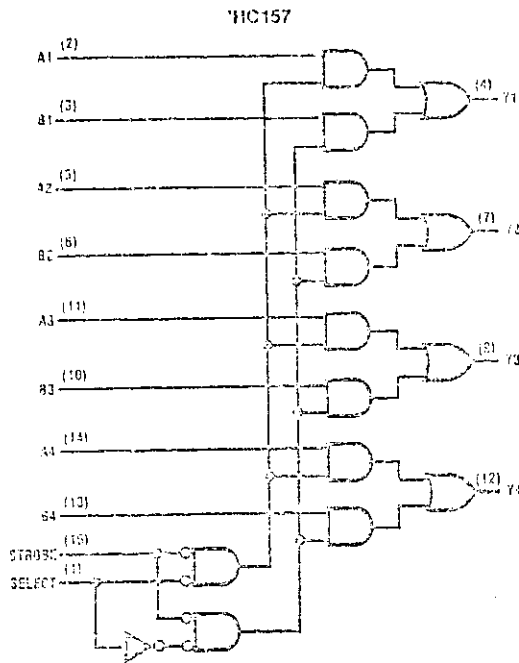
Parameter	Conditions	Typ	Guaranteed Limit	Units
Maximum Propagation Delay, Data to Output		14	20	ns
Maximum Propagation Delay, Select to Output		14	20	ns
Maximum Propagation Delay, Inhibit to Output		12	18	ns

Electrical Characteristics C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

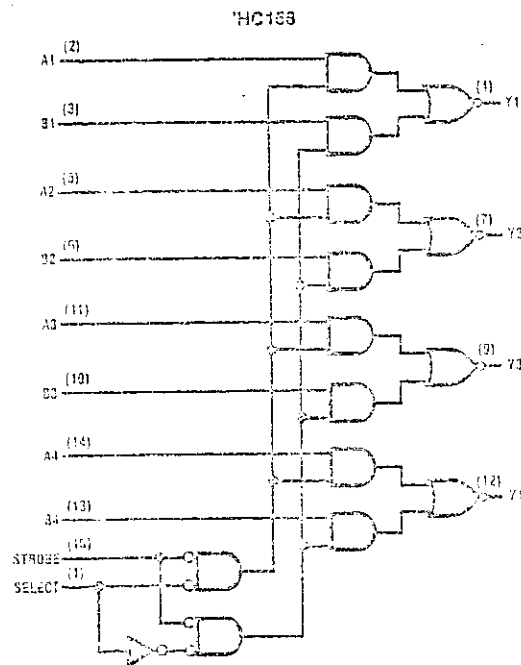
Parameter	Conditions	V _{CC}	T _A = 25°C		74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C	Units
			Typ	Guaranteed Limits			
Maximum Propagation Delay, Data to Output		2.0V	63	125	153	186	ns
			4.5V	13	25	32	37
			6.0V	11	21	27	32
Maximum Propagation Delay, Select to Output	*	2.0V	63	125	158	186	ns
			4.5V	10	25	32	37
			6.0V	11	21	27	32
Maximum Propagation Delay, Strobe to Output		2.0V	58	115	145	171	ns
			4.5V	13	23	29	34
			6.0V	10	20	25	29
Maximum Output Rise and Fall Time		2.0V	30	75	55	110	ns
			4.5V	8	15	19	22
			6.0V	7	13	16	19
Maximum Input Capacitance			5	10	10	PF	
Power Dissipation (per Multiplexer)						PF	

* Selects the no load dynamic power consumption, P_D = C_{IN} V_{CC}² f + C_{OUT} V_{CC} and the no load dynamic current consumption, I_S = C_{IN} V_{CC} f + I_{CC}

Logic Diagrams



TL/F/5314-3



TL/F/5314-4

National Semiconductor

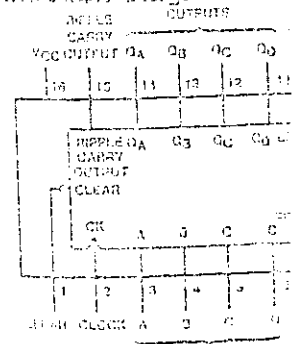
MM54HC150/MM74HC150
 4-Bit Binary Counter with
 MM54HC151/MM74HC151
 4-Bit Binary Counter with
 MM54HC152/MM74HC152
 4-Bit Binary Counter with
 MM54HC153/MM74HC153
 4-Bit Binary Counter with
 Internal Description

MM54HC150/MM74HC150, MM54HC151/MM74HC151, MM54HC152/MM74HC152, and MM54HC153/MM74HC153 synchronous counters using CMOS Technology, 0.5 μ m process, and internal look-ahead carry for high speed counting applications. They offer high speed and low power consumption in a package similar to low power Schottky TTL. MM54HC152 are 4 bit decade counters. MM54HC153 are 4 bit binary counters. All counters are clocked simultaneously on the low to high transition of the CLOCK input waveform.

These counters may be preset using the LOAD input. The output of all four flip-flops is synchronous with the CLOCK. When LOAD is held low, counter outputs on the A, B, C, and D inputs will be preset on the rising edge of CLOCK. If LOAD is high before the positive edge of CLOCK, the counter will be unaffected.

These counters may be cleared by the CLEAR input. The clear function on the MM54HC150, MM54HC152, and MM74HC153 counters is active low. That is, the counters are cleared on the falling edge of CLOCK when the clear input is low.

Connection Diagram



DATA SHEET

Order Number MM54HC150, MM54HC151, MM54HC152, MM54HC153, and MM74HC150, MM74HC151, MM74HC152, MM74HC153. See NS Package J18A for details.

Especificações Técnicas do IC 16 - 74LS02 -

Absolute Maximum Ratings (Notes 1, 2)

Supply Voltage (V _{CC})	-0.5V to 7.0V
DC Input Voltage (V _{IN})	-1.5 to V _{CC} + 1.5V
DC Output Voltage (V _{OUT})	-0.5 to V _{CC} + 0.5V
Clamp Diode Current (I _{CL} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V _{CC} or GND Current, per pin (I _{CC})	±50 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D) (Note 3)	500 mW
Lead Temperature (T _L)	260°C
(Soldering 10 seconds)	

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C	74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C
V _{IH}	Maximum High Level Input Voltage		2.0V	Typ	1.5	1.5
				Guaranteed Limits	3.15	3.15
					4.2	4.2
V _{IL}	Maximum Low Level Input Voltage		2.0V	Typ	0.3	0.3
				Guaranteed Limits	0.9	0.9
					1.2	1.2
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	Typ	1.9	1.9
				Guaranteed Limits	4.4	4.4
					5.9	5.9
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	Typ	0.53	0.54
				Guaranteed Limits	5.2	5.34
					5.48	5.2
I _{OH}	Maximum Output Current	V _{IN} = V _{IL} I _{OUT} ≤ 20 μA	2.0V	Typ	0	0.1
				Guaranteed Limits	0.1	0.1
					0.1	0.1
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{IL} I _{OUT} = 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	Typ	0.2	0.4
				Guaranteed Limits	0.25	0.4
					±1.0	±1.0
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	6.0V	Typ	±0	±0
				Guaranteed Limits	±0	±0

Note 1: The maximum range and the value of V_{CC} are defined by the device type.

Note 2: Power dissipation is calculated by the following equation:

$$P_D = (V_{CC} - V_{OH}) I_{OH} + (V_{OH} - V_{OL}) I_{OL} + V_{CC} I_{CC}$$

Note 3: Power dissipation is calculated by the following equation: P_D = C_{IN} V_{CC} f + C_{OUT} V_{CC} f + C_{LOAD} V_{CC} f + C_{LOAD} V_{OUT} f. The values of C_{IN}, C_{OUT}, and C_{LOAD} are 10 pF, 10 pF, and 10 pF, respectively. The values of f are 10 MHz, 10 MHz, and 10 MHz, respectively. The values of V_{CC} and V_{OUT} are 5.0V and 5.0V, respectively. The value of C_{LOAD} is 5.0 pF. The value of C_{LOAD} is 5.0 pF.

Note 4: The values of V_{IH} and V_{IL} are defined by the following equation: V_{IH} = 0.7 V_{CC} and V_{IL} = 0.3 V_{CC}.

Parameter	Typ	74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C
Propagation Delay	50	125	150
Maximum Output Rise and Fall Time	12	25	30
Power Dissipation (per gate)	9	21	25
Maximum Input Capacitance	50	95	110
Maximum Input Capacitance	5	10	10

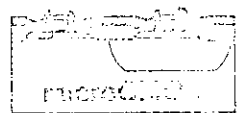
AC Characteristics

Parameter	Conditions	V _{CC}	T _A = 25°C	74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C
Propagation Delay		2.0V	Typ	50	150
			Guaranteed Limits	12	25
				9	21
Maximum Output Rise and Fall Time		2.0V	Typ	50	110
			Guaranteed Limits	6	22
				7	19
Power Dissipation (per gate)		6.0V	Typ	50	10
			Guaranteed Limits	5	10
				5	10

Note 1: The values of V_{IH} and V_{IL} are defined by the following equation: V_{IH} = 0.7 V_{CC} and V_{IL} = 0.3 V_{CC}.

Note 2: Power dissipation is calculated by the following equation: P_D = C_{IN} V_{CC} f + C_{OUT} V_{CC} f + C_{LOAD} V_{CC} f + C_{LOAD} V_{OUT} f. The values of C_{IN}, C_{OUT}, and C_{LOAD} are 10 pF, 10 pF, and 10 pF, respectively. The values of f are 10 MHz, 10 MHz, and 10 MHz, respectively. The values of V_{CC} and V_{OUT} are 5.0V and 5.0V, respectively. The value of C_{LOAD} is 5.0 pF. The value of C_{LOAD} is 5.0 pF.

LS14549C/LS14549D/LS14549E
Quad Input OR Gate



LS14549C/LS14549D/LS14549E
Quad Input OR Gate

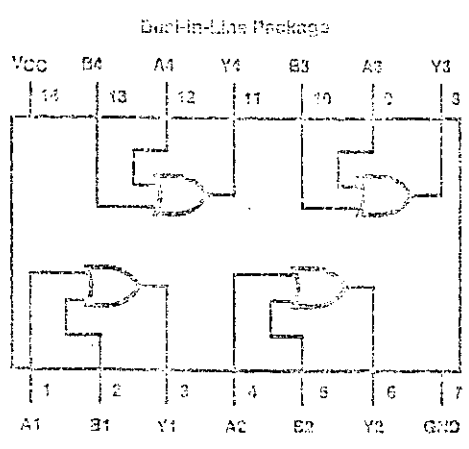
General Description

This device utilizes micro-DMOS Technology, a first generation process CMOS, to achieve operating speeds similar to TTL gates with the low power consumption of CMOS. The integrated circuit consists of four buffered OR gates with high noise immunity and the ability to drive TTL loads. The LS14549C/LS14549D logic family is particularly well suited for use in applications where the standard 54HC/74HC family is not available. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and GND.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2-6V
- Low quiescent current: 20 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads

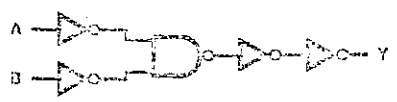
Connection and Logic Diagrams



TL/F/5132-1

Top View

Order Number 81549C32J or 81549D32J
 See I/O Package J14A or N14A



$Y = A + B$

TL/F/5132-2

Inputs otherwise specified

54HC	74HC
220	110
49	22
42	19
10	

no current consumption, Ig = 0, V_{CC} = V_{OL}

Especificações Técnicas das Rams - 4416NL -